

# VLSI Design

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## Outline

1. Element Design Guides
2. Process Errors and Matched Layout
3. Switch Characteristics
4. CMOS Gate Transistor Sizing
5. Power Dissipation
6. Conductor Sizing
7. Charge Sharing
8. Design Margining
9. Yield

## Channel Sheet Resistance

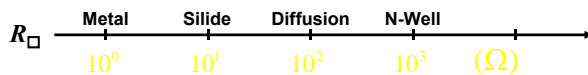
- Linear Region: VCR (Voltage Control Resistance) Region.

**Linear Region:**  $I_{DS} = \beta \left[ (V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2} \right]$

$$R \equiv \frac{\delta V_{DS}}{\delta I_{DS}} = \frac{1}{\mu C_{ox}(V_{GS} - V_T - V_{DS})} \cdot \frac{L}{W} \approx \frac{1}{\mu C_{ox}(V_{GS} - V_T)} \cdot \frac{L}{W}$$

**Channel Sheet Conductance**  $\sigma_s \approx \mu C_{ox}(V_{GS} - V_T)$

- Approximate Orders in about 2000's Technologies:



## Approximate Intrinsic MOS Gate $C_{\square}$

$C_g =$

Region Portion	Cut-off	Linear	Saturated
$C_{gb}$	$\frac{\epsilon A}{t_{ox}}$	0	0
$C_{gs}$	0	$\frac{\epsilon A}{2t_{ox}}$	$\frac{2\epsilon A}{3t_{ox}}$
$C_{gd}$	0	$\frac{\epsilon A}{2t_{ox}}$	0

$$C_{\square} = 1 \sim 10 \text{ fF}/\mu\text{m}^2$$

## Element Design Guide

### Resolution/Error

- **Spiral Inductance:** > 10%
- **Resistance:** about 5% ~ 10%
- **Poly-capacitance:** about 1%
- **Error cancellation is usually used to reduce the error from about 10% to 1%.**
- **Fit the range in non-critical circuit then take care of the resolution in critical circuit.**

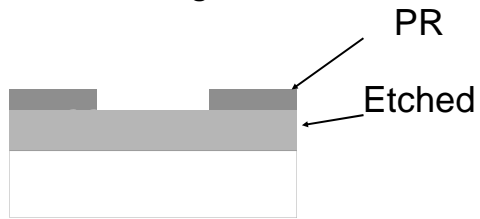
## Process Error

### Process Error

- **Geometrical Factor**
  - XY-Plane: Shifting
  - Z-Plane: usually radial to the aperture
- **Non-Geometrical Factor**
  - Density, temperature, duration, defect, etc.

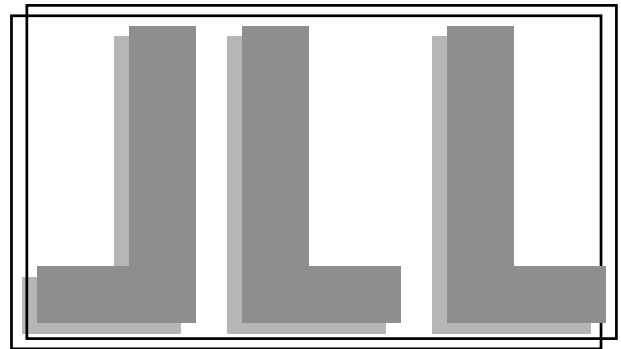
## Geometrical Errors

1. Radical factor : e.g.,

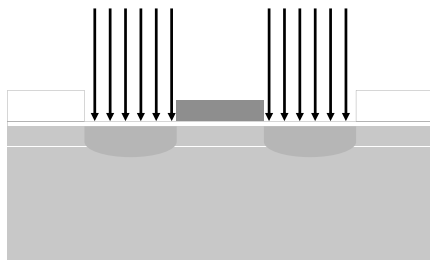


## Geometrical Errors

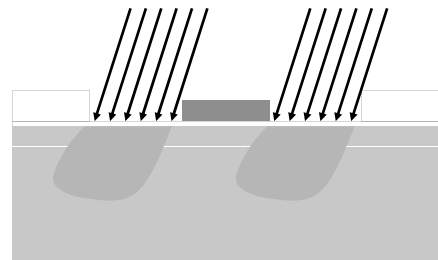
2. Shifting : e.g.,



## Optimized Angle of Iron Implant



## Optimized Angle of Iron Implant



The implant parameters and the yield will be traded off.

## Matching



## Matching for Constant Errors



$$\frac{w+\Delta w}{L+\Delta L}$$

$$\frac{w+\Delta w}{L+\Delta L}$$

### Matching for Gradient Errors

$2\omega_2 = \omega_1 + \omega_3$

$\Delta W = \omega_1$

$\Delta W = \omega_3$

T.-C. Huang, NCUE Fall 2011 Page 13

### Ratio-Matching

1. Duplication :

T.-C. Huang, NCUE Fall 2011 Page 14

### Ratio-Matching

2. E.g., Current repeater:

MA	g	g	v	v	pch	W=1u	L=1u	
MB	d	g	v	v	pch	W=2u	L=1u	
MA	g	g	v	v	pch	W=1u	L=1u	
MB1	d	g	v	v	pch	W=1u	L=1u	
MB2	d	g	v	v	pch	W=1u	L=1u	
MA	g	g	v	v	pch	W=1u	L=1u	
MB	d	g	v	v	pch	W=1u	L=1u	M=2

T.-C. Huang, NCUE Fall 2011 Page 15

### Ratio-Matching

3. E.g., Voltage divider :

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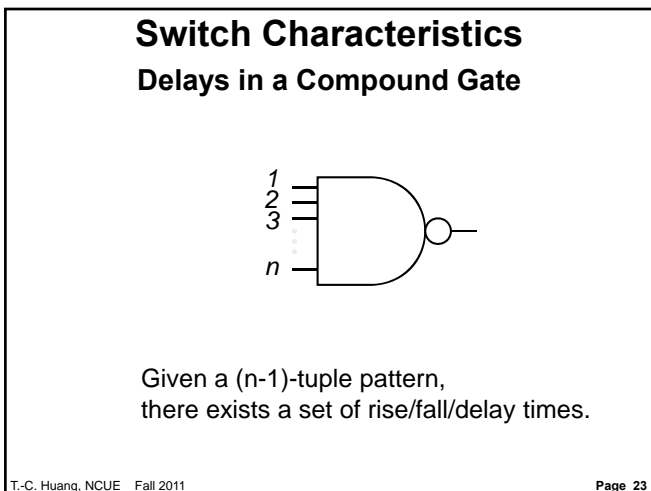
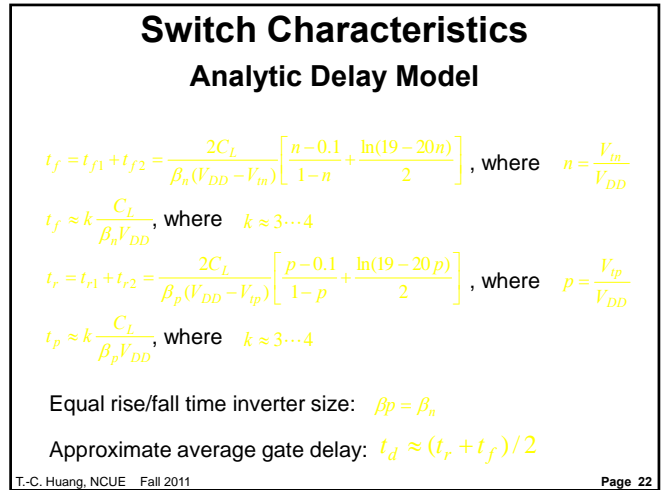
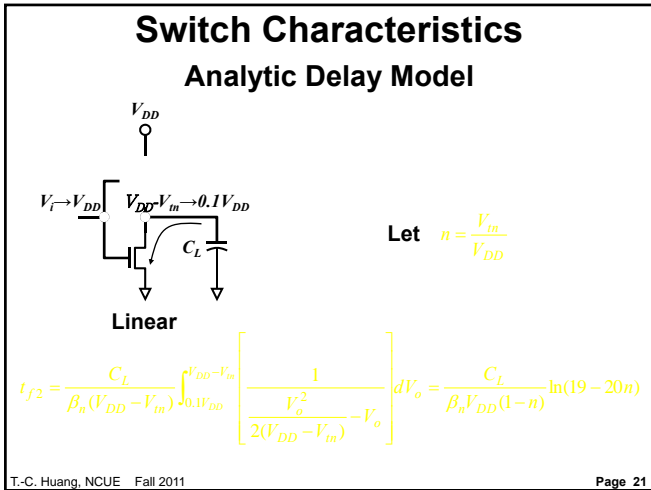
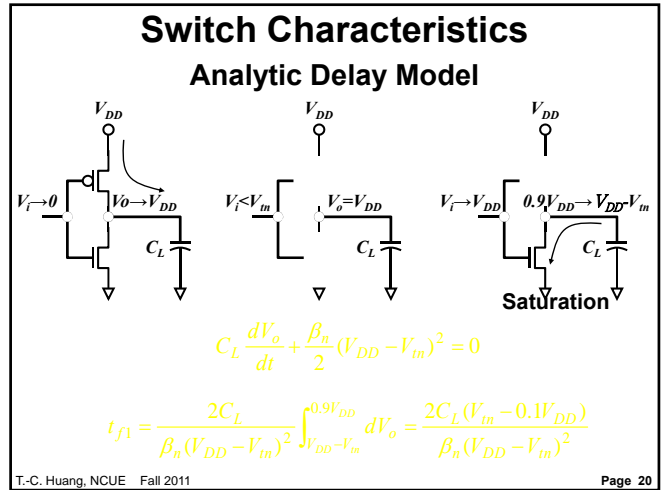
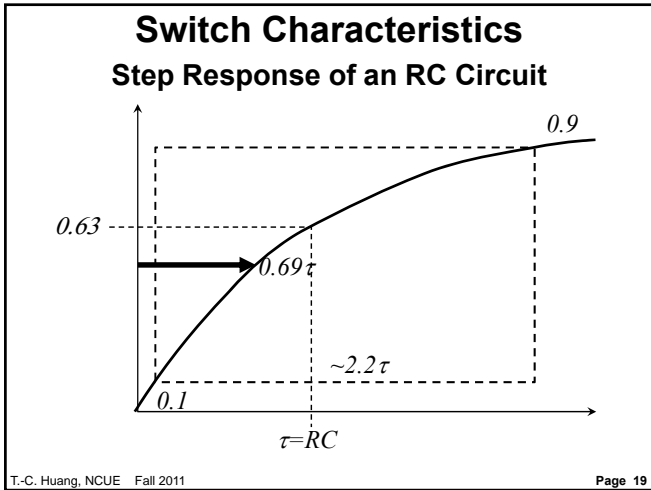
### Switching Timing Parameters

1. Rise Time:  $0.1V_{dd} \rightarrow 0.9V_{dd}$
2. Fall Time:  $0.9V_{dd} \rightarrow 0.1V_{dd}$
3. Delay:  $0.5V_{dd}$  Input  $\rightarrow$   $0.5V_{dd}$  Output  
??? for a single gate or with a cascade delay line ?
4. Propagation Time :  
Input change starting  $\rightarrow$  Output steady
5. Settling Time:  
Change starting  $\rightarrow$  (Error < allowance)  
Note to justify for given premise.

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### Switching Timing Parameters

T.-C. Huang, NCUE Fall 2011 Page 18

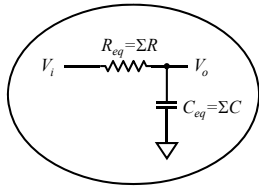


### Transistor-Level Models

No	Model	Nmemonics	Examples
1	Switch	$R_{off} = \infty$	M1 on $\rightarrow$ M2 off $\rightarrow$ Vo=Vdd
2	Stack Effect	$R_s = \sum R_i$	Wafer Power, Equivalent R
3	RC Model	$\tau = RC$	$T_r = 2.2\tau$ , $t_f = 0.69\tau$ , $f = 1/2\pi\tau$
4	Toggle Rate	$Pd = ka$	$a = \text{switching activity}$
5	EI More Model	$\tau = \sum (RC)_{loop}$	Intrinsic Delay, $T_r$ , $T_d$ , $P_d$ , gate parameters
6	Rabaey's Logical Effort	$i + bl$	$P_d$ , $T_p$ of gate-level circuits
7	Shocklay	1 <sup>st</sup> Order Eq.	See Lec.3
8	SPICE II	-	See Lec.4
9	BSIM	-	Refer to ucb

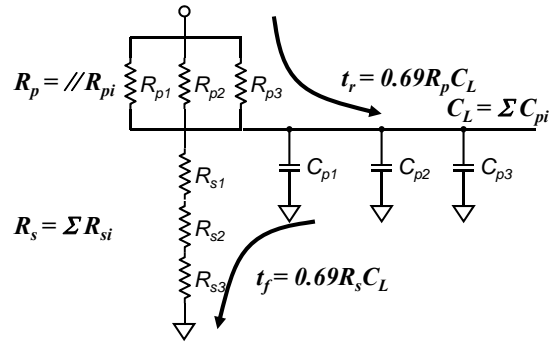
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## Switch Characteristics Worst-Case RC Model

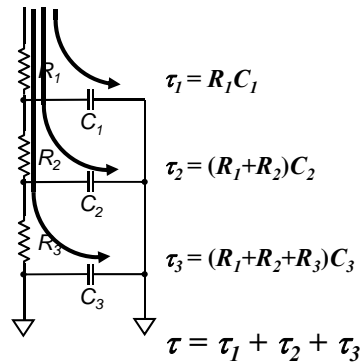


$$\text{Time Constant} = \tau < R_{eq} C_{eq}$$

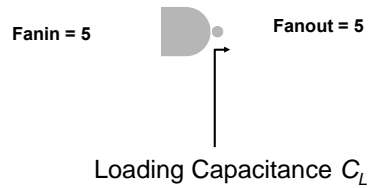
## Simple RC Model – Stack Effect



## Elmore Delay Model

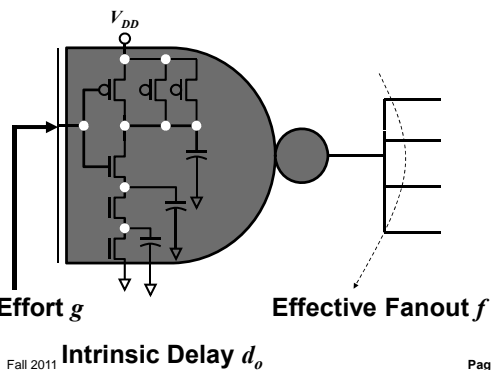


## Switch Characteristics Loading



## Efforts of Gate Delay

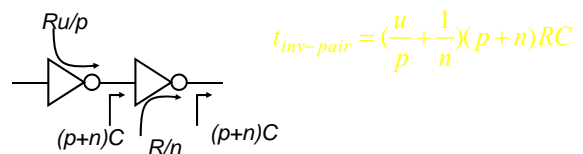
$$t_d = gf + d_o$$



## Gate Transistor Sizing Cascade CMOS Inverters

For an inverter with  $L_p=L_n=L_{min}$ , and  $W_p=pW_{min}$ ,  $W_n=nW_{min}$ :

Let  $C=C_L$  when  $W_p=W_n=W_{min}$ ,  
 $R=R_n$  when  $W_p=W_n=W_{min}$  and  
 $\mu_p:\mu_n=u:1$

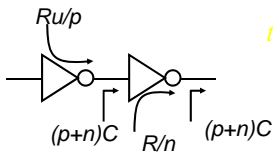


If  $u=2$ , then it has the same delay for  $p=n$  and  $p=2n$ .

## Gate Transistor Sizing

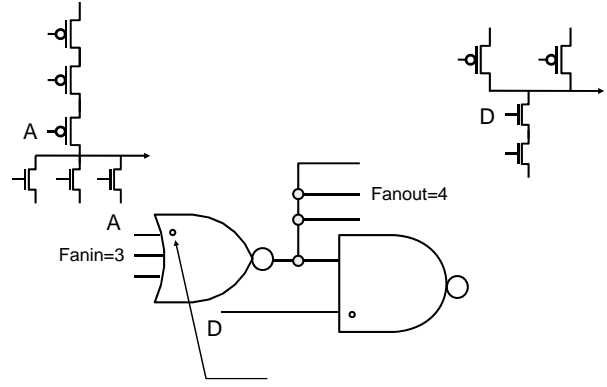
### Cascade Psuedo-NMOS Inverters

For equivalent noise margin (ENM) pseudo-NMOS inverters:  
 $\beta_n/\beta_p \approx 6$ , such that  $n=3p$  is usually chosen.



$$t_{inv-pair} = \left(\frac{u}{p} + \frac{1}{n}\right)(p+n)RC$$

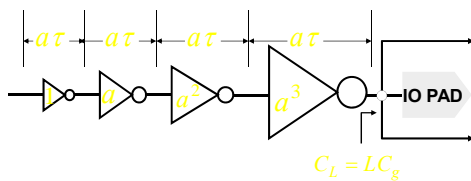
## Fan-In and Fan-Out



To that nearest to output in the serial transistors

## Gate Transistor Sizing

Stage Ratio  $a$

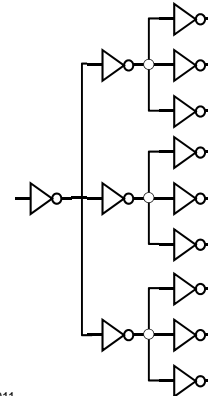


Total delay =  $n a \tau = \frac{\ln(L)}{\ln(a)} a \tau$  To minimize  $\frac{a}{\ln(a)}$ , we have  $a = e \approx 2.72$



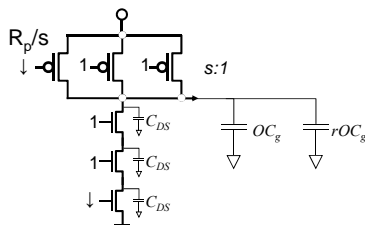
## Clock Tree

using Standard Cells with a Stage Ratio 3



## Transistor Stage-Ratio Principle

Assume size:  $s$ ,  $C_{DS} = dC_g$ ,  $C_{l-route} = rC_g$  and  $Fanin = I$ ,  $Fanout = O$



$$t_r = (R_p/s)[(sId + rO + O)C_g]$$

$$t_f = (IR_n/s)[(sId + rO + O)C_g]$$

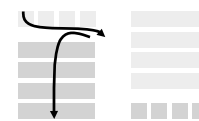
output part  
 internal part

## Transistor Stage-Ratio Principle

### Equal Rise/Fall Time Design

If  $t_r = t_f$ ,  $\mu_p W_p = I \mu_n W_n$  for NAND gates

$I \mu_p W_p = \mu_n W_n$  for NOR gates.



Normalized-mobility

Usually,  $I \approx 2 \dots 5$

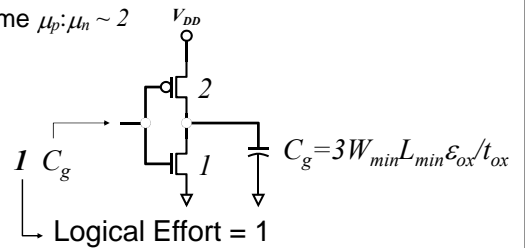
## Transistor Stage-Ratio Principle

High-Speed Design Guideline

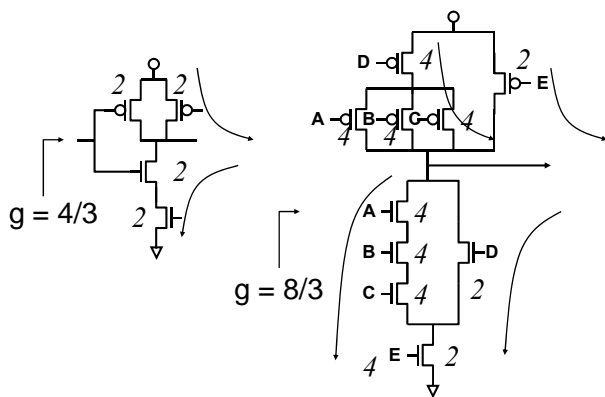
1. Use NAND instead of NOR gates
2. Place inverters at high-fanout nodes
3. Fanin < 5; Fanout < 10
4. Use min.-sized gates on high-fanout nodes;
5. Keep Rise/Fall edges sharp

## Logical Efforts

- Usually, select input capacitance  $C_g$ , turn-on resistance  $R_{on}$  as units.
- Mark the transistor widths in units  $W_{min}$  when all  $L$ 's =  $L_{min}$
- Assume  $\mu_p: \mu_n \sim 2$

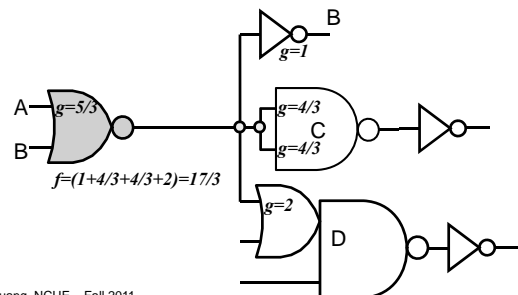


## Examples for Logical Efforts



## Effective Fanout $f$

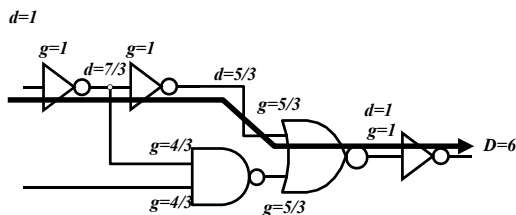
Neglecting intrinsic delay,  $t_r=1$   $f=1$   $g=1$  Named as invhx  
 Assume the unitary inverter has a half drive for driving 2 inverters.



## Example: Unitary-Drive Design

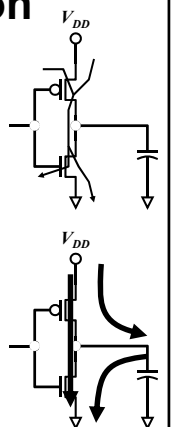
$t_r=1$   $f=1$   $g=1$

Neglecting intrinsic delay, Named as invhx  
 Assume the unitary inverter has a half drive for driving 2 inverters.

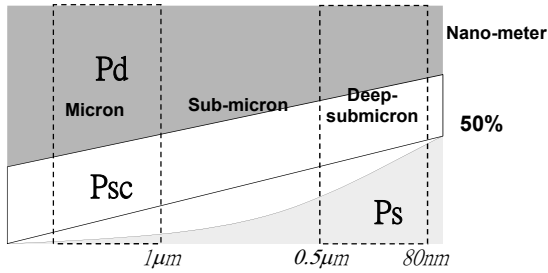


## Power Dissipation

- Static Power Dissipation
- Dynamic Power Dissipation
  - Switching Transient (Short-circuit) Current
  - Charging/Discharging of  $C_L$



# Power Dissipation



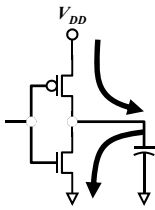
# Power Dissipation

## Static Dissipation

- **Quiescent State**
  - Input steady for enough time
  - Either P- or N- Network is off
  - Theoretically,  $IDDQ \rightarrow 0$
- **However, small static dissipation due to**
  - Reverse bias leakage  $I_{SB}$
  - Gate leakage
- **Considerable in deep submicron era**

# Power Dissipation

## Dynamic Dissipation



$$P_d = \frac{1}{T} \left[ \int_0^{T/2} i_n(t) V_o dt + \int_{T/2}^T i_p(t) (V_{DD} - V_o) dt \right]$$

$$\therefore i(t) dt = C dV$$

$$\therefore P_d = C_L V_{DD}^2 f_p$$

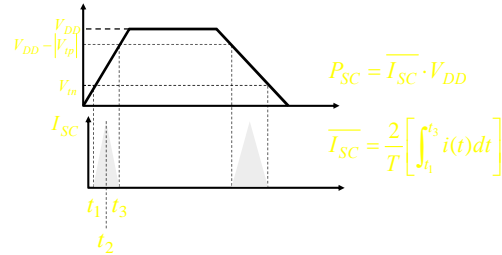
Note  $f_p$  is a repetition frequency

For CMOS Logic Circuits with switching activity  $a$ , select circuit frequency  $f = f_p a$ ;

$$P_d = \frac{1}{2} a f C_L V_{DD}^2$$

# Power Dissipation

## Short-Circuit Dissipation



$$P_{SC} = \overline{I_{SC}} \cdot V_{DD}$$

$$\overline{I_{SC}} = \frac{2}{T} \left[ \int_{t_1}^{t_3} i(t) dt \right]$$

Under linear approximation  $t_r = t_f = rT$  and  $V_{in} = |V_{op}| = V_t$ ,

$$P_{SC} = \frac{\beta r}{12} (V_{DD} - 2V_t)^3$$

# Over-dissipation

## 1. Conductor Damage

### 1. Metal Migration

1.  $J < J_{max}$  ← Contact Replication
2. Temperature
3. Crystal structure

### 2. Noise & Crosstalk

### 3. RC Delay

## 2. Ground (Power) Bounce

1. Performance Impact
2. Failure

# Measurement in HSPICE

- TRAN 1PS 1US
- MEAS TRAN P1 AVG POWER FROM=10NS TO=40NS
- MEAS TRAN P2 RMS POWER
- MEAS TRAN T1 TRIG V(IN) VAL=2.5 RISE=1
- + TARG V(OUT) VAL=2.5 FALL=1

In file.lis, you can find the report of P1, P2, and T1.