VLSI Design

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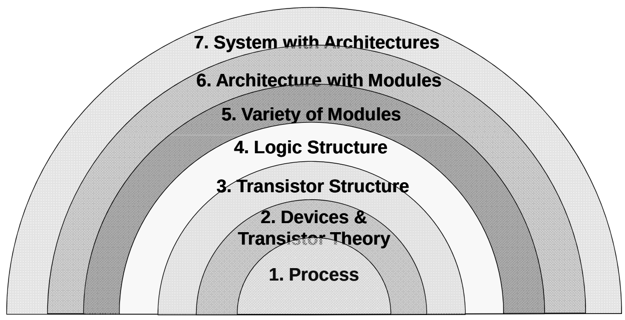
Syllabus Structure

Bottom-up Hierarchy



Notes

Before Class

- Question and Answer in English
  - ✓ Ask a question in English about last lesson.
- 10-minute Quiz
  - ✓ Answer a 10-minute quiz
  - ✓ Evaluate and correct by each other
  - ✓ Try to answer in English

MOS Transistor Theory

Basic Semiconductor Devices in MOS Process

- Resistance
  - ✓ Metal, Silicide, Poly, Diffusion, Well, Chanel
- Coil Inductor
  - ✓ Spiral Metal
- Plate Capacitor
  - ✓ Metal Poly, Poly-Poly, Poly-Substrate, Chanel
- MOS Transistor
  - ✓ V-I Characteristics/Modeling
  - ✓ Pass Transistor Operation
  - ✓ Chanel Resistance
  - ✓ Gate Capacitance
  - ✓ Transistor Diode
  - ✓ Pass Transistor and Switch

MOS Transistor Theory

Usual Semiconductor Elements in MOS Process

- Wire Resistance
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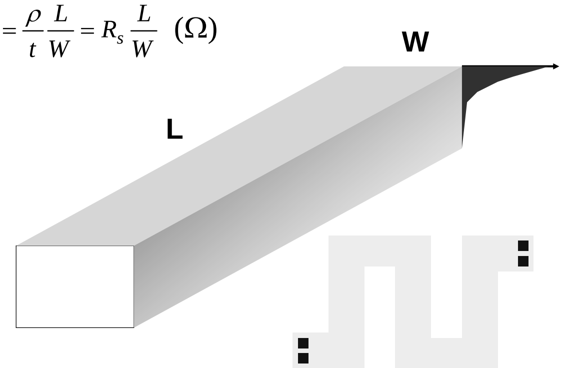
Sheet Resistance

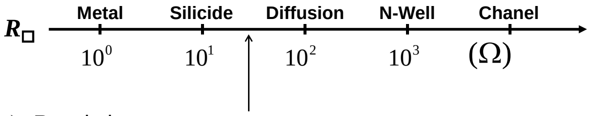
$$R = \frac{\rho}{t}\frac{L}{W} = R_s \frac{L}{W} \quad (\Omega)$$



e.g., Polysilicon resistor, diffusion resistor

Wire Sheet Resistance

- Approximate Orders in about 2000's Technologies:



- Resolution: **Polysilicon ➔ about 1% error**
  - ✓ **Polysilicon is usually the best wire sheet resistor for accurate resistance.**
- Heat Radiation: In a 5-face adiabatic model,

$$\mathrm{H} \propto \mathrm{A} = WL$$

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Coil Inductor

- **Cylindrical air-core coil:**

$$\mathrm{L} = \frac{\mu k N^2 A}{l} \ \text{(Henries, H)} \qquad \begin{cases} \mathrm{N}: \# \text{ turns} \\ A: \text{ Area} \\ l: \text{ length} \end{cases}$$

- **Flat Spiral Inductor:**

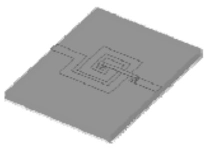

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Plate Capacitance

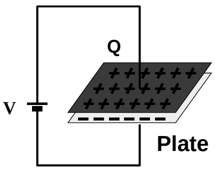
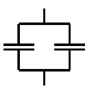
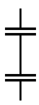


Plate Capacitance: $C \equiv \frac{Q}{V} = \varepsilon \frac{A}{t}$

Area, **Permittivity**, **Thickness**



C=C1+C2



$$C = \frac{1}{\frac{1}{C_1} + \frac{1}{C}}$$

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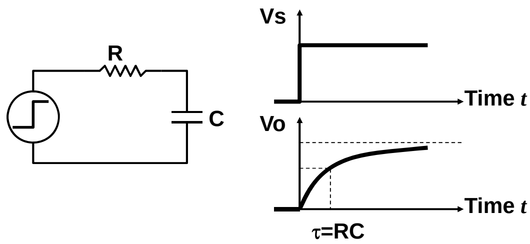
First Order Time Constant



Charging Energy: $\frac{1}{2} C V^2$

Nothing to do with R!

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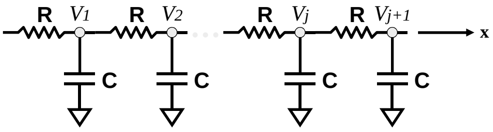
Transmission Line Effect



$$C\frac{dV_j}{dt} = (I_{j-1} - I_j) = \frac{V_{j-1} - V_j}{R} - \frac{V_j - V_{j+1}}{R}$$

$$rc\frac{\delta V}{\delta t} = \frac{\delta^2 V}{\delta x^2}$$ **, where** $r = \frac{\delta R}{\delta x}$ **and** $c = \frac{\delta C}{\delta x}$

It's a wave function,
and the propagation time for step response:

$$t_x = kx^2$$

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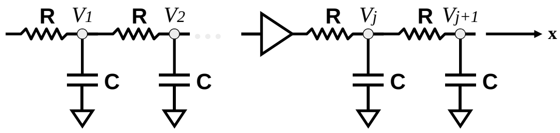
Transmission Line Effect

Approximate propagation time: $t_n = \frac{RCn(n+1)}{2}$

One solution to reduce the propagation time:
Adding buffers:



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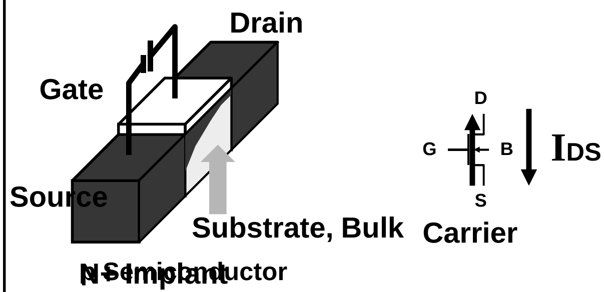
An n-Type MOS Transistor



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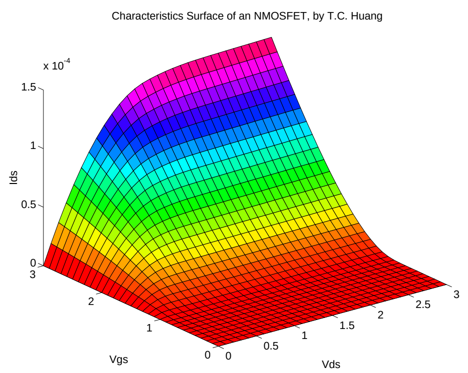

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Levelized Power/Timing Models

- ✓ **RTL Level and Models as Heuristics**
  - **Transition count model,**
  - **Imax,**
  - **Charge model as Thermal model, etc.**
- ✓ **Logic Level and Speedup Model**
  - **Switching model,**
  - **RC Model,**
  - **Elmore Model**
- ✓ **Manual Model**
  - **First-order equations**
  - **Lambda Rules for Voltage Scaling**
- ✓ **SPICE Model**
  - **Level 1 (simple dc)**
  - **Level 2 (modified)**
  - **Level 3 (+ Empirical short-channel)**
  - **Level 4 (BSIM)**
- ✓ **Physics and Electronics Levels**
  - **Physics and Electronics Theories, MOS Model, BJT Model, p model**

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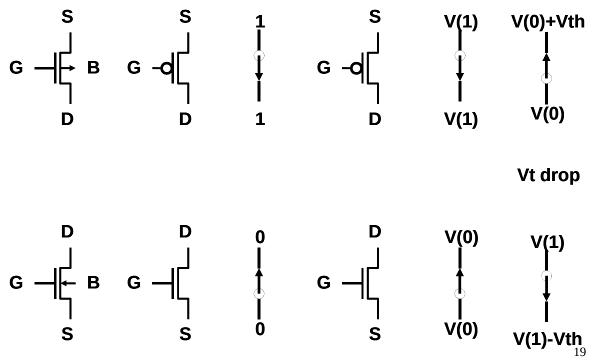
Switch Intention



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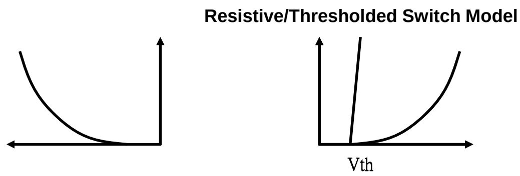
Simple Switch Model of an n-MOSFET



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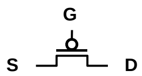
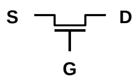
Pass Transistor as Switch

1. Good p/n switch for 1/0 but bad for 0/1
2. CMOS Transmission gate – another compensated structure



3. Pass Transistor Logic (PTL)
   1. VDD >> stages * Vth
   2. Pulled-up or down



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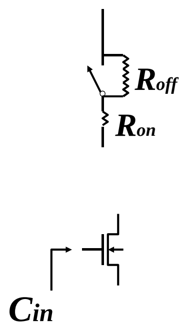
RC Switch Model



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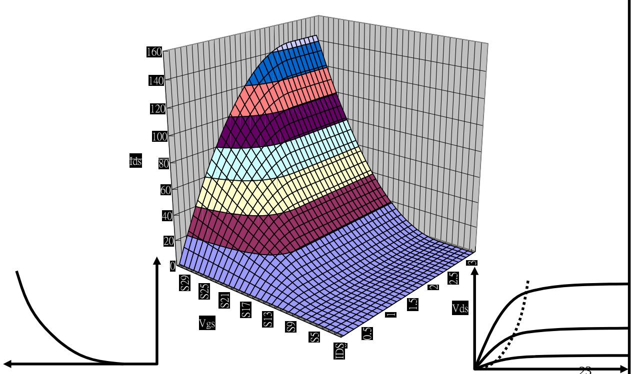
Measured Characteristics of a MOSFET



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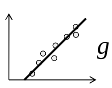
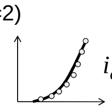
Useful Regressions

- Linear Regression (α=1)
  - ✓ First-Order Equation



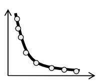
$$g_m = k(v_{gs} - v_t)$$

- Second-Order Regression (α=2)
  - ✓ Parabolic Regression



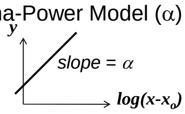
$$i_{ds} = k(v_{gs} - v_t)^2$$

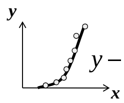
- Hyperbolic Regression (α=-1)



$$R_s(v_{gs} - v_t) = k$$

- Alpha-Power Model (α)





$$y - y_o = (x - x_o)^\alpha$$

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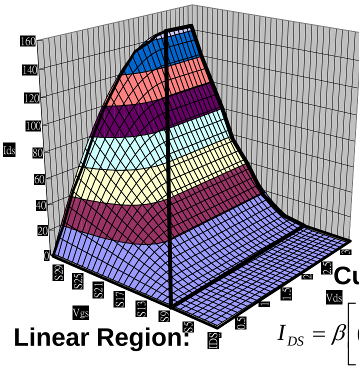
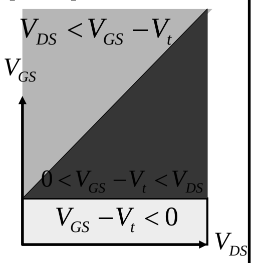
First Order (Shocklay) Equations





Cut-Off Region: $I_{DS} = 0$

Linear Region: $I_{DS} = \beta\left[(V_{GS} - V_t)V_{DS} - \frac{V_{DS}^2}{2}\right]$

Saturation Region: $I_{DS} = \frac{\beta}{2}(V_{GS} - V_t)^2$

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MOS Transistor Gain Factor β

$\mu_p \approx 200cm^2/(V \cdot \sec)$

$\mu_n \approx 500cm^2/(V \cdot \sec)$

Mobility

Gate Oxide Capacitance $C_{ox} \equiv \frac{\varepsilon}{t_{ox}}$

$\approx 4\varepsilon_o$

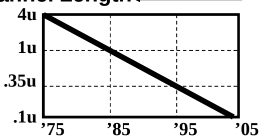
Channel Width

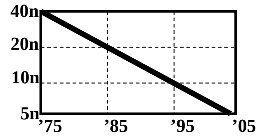
Permittivity

$$\beta = K\frac{W}{L} = \frac{\mu\varepsilon}{t_{ox}}\frac{W}{L}$$

Channel Length

Oxide Thickness





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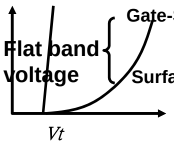
Threshold Voltage

$V_t = V_{t-mos} + V_{fb}$



Flat band voltage { **Gate-Substrate Work Function**, **Surface State Charge** }

doping t_o

MOS Capacitor Threshold Voltage { **Oxide Capacitance**, **Bulk Charge Term** }

Usually, while the process technology is fixed,
VLSI Layout Engineers can only take care of *VB* and T (temperature).

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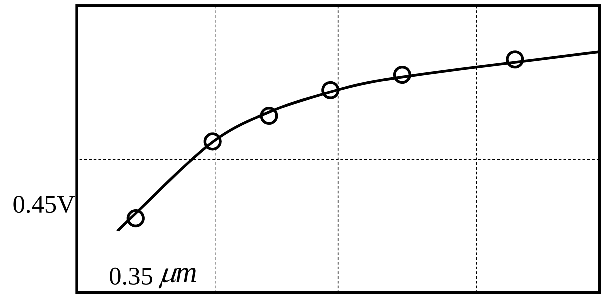
Threshold Voltage Changing due to Short Channel



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Threshold Voltage Changing due to Bulk Voltage

$$|V_t| = |V_{to}| + \Delta V_t$$

$$\Delta V_t \approx \gamma(\sqrt{2\Phi_F + V_B} - \sqrt{2\Phi_F})$$

$$\Delta V_t << 2\Phi_F \qquad \Delta V_t \approx \gamma\sqrt{V_B}$$

(A Typical value of γ is about 0.6)

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Channel Sheet Resistance

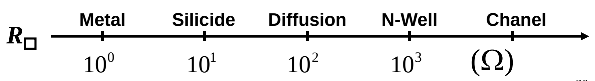
- Linear Region: VCR (Voltage Control Resistance) Region.

Linear Region: $I_{DS} = \beta\left[(V_{GS} - V_t)V_{DS} - \frac{V_{DS}^2}{2}\right]$

$$R \equiv \frac{\delta V_{DS}}{\delta I_{DS}} = \frac{1}{\mu C_{ox}(V_{GS} - V_t - V_{DS})} \cdot \frac{L}{W} \approx \frac{1}{\mu C_{ox}(V_{GS} - V_t)} \cdot \frac{L}{W}$$

Channel Sheet Conductance $\sigma_s \approx \mu C_{ox}(V_{GS} - V_t)$

- Approximate Orders in about 2000's Technologies:



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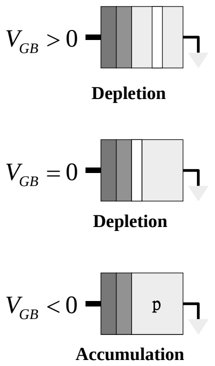
MOS Capacitance



Low Frequency / **High Frequency**

Gate Capacitance: $C \equiv \dfrac{C_{SiO_2} C_{dep}}{C_{SiO_2} + C_{dep}}$

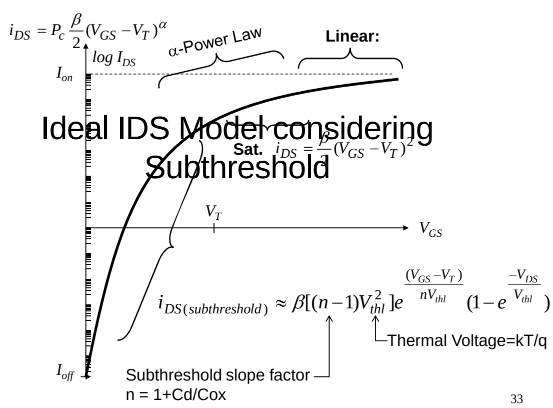
Oxide Capacitance: $C \equiv \dfrac{\varepsilon_{SiO_2}\varepsilon_o}{t_{ox}} A$

Approximate Intrinsic MOS Gate C□

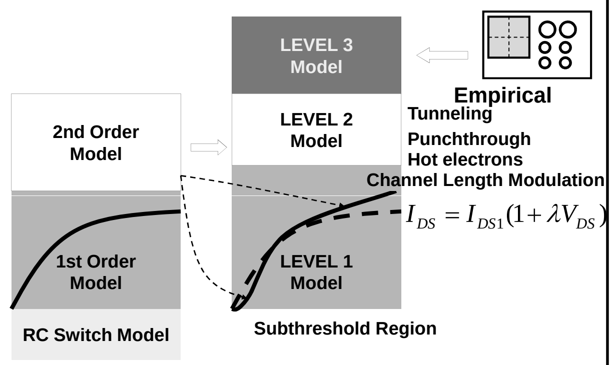
***Cg* =**

Region / Portion	Cut-off	Linear	Saturated
C_{gb}	$\frac{\varepsilon A}{t_{ox}}$	0	0
C_{gs}	0	$\frac{\varepsilon A}{2t_{ox}}$	$\frac{2\varepsilon A}{3t_{ox}}$
C_{gd}	0	$\frac{\varepsilon A}{2t_{ox}}$	0

Ideal IDS Model considering Subthreshold



SPICE Modeling



Transistor Power/Timing Models

Summary

- Switch Models
  - ✓ Ideal Switch: Functional simulation without timing
  - ✓ Resistive Switch: Static power evaluation
  - ✓ Capacitive Switch: Dynamic power evaluation
  - ✓ RC Switch: Basic power and timing evaluation
- Transistor Structure Model
  - ✓ El More Model: loop RC additive.
  - ✓ Rabaey Model: Logical and branch efforts
- IDS Models
  - ✓ Shockley First-Order Equation: accurate manual derivation
  - ✓ Sub-threshold Models
- SPICE Models
  - ✓ Complicate Simulation

Transistor Network

Relay Logics

- **Stack Effect**
  - ✓ Parallel Switch: $S_{on} = A_{on} + B_{on}$, $R_s = R_A // R_B$
  - ✓ Serial Switch: $S_{on} = A_{on} \cdot B_{on}$, $R_s = R_A + R_B$
  - ✓ Parallel Capacitors: $C = C_A + C_B$
- **Body Effect**
  - ✓ is the threshold voltage changing of source-bulk voltage due to transistor connection in series.

$$V_{t2} \approx V_{t2} + 0.6\sqrt{V_{D1}}$$