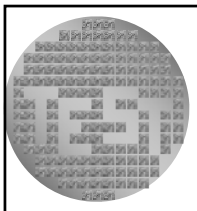

VLSI Design

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2011/12/05

Clocking Strategies

1. Clocked System
2. Latch and Registers
3. System Timing (Constraint)
4. Single-Phase Memory
5. Phase Locked Loop Clock Techniques
6. Metastability and Synchronization Failure
7. Single-Phase Logic Structure
8. Two-Phase Clocking
9. Two-Phase Memory Structure
10. Two-Phase Logic Structures
11. Four-Phase Clocking
12. Four-Phase Memory Structures
13. Four-Phase Logic Structures
14. Clock Distribution

Clocking Strategies

Clocked System

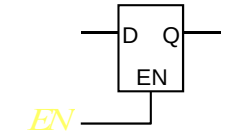
Considerations:

- Independent Clock Count
- Clock phase count for each independent clock
- Clock domains
- Synchronous or Asynchronous
- Clock-Generator: Jitter
- Distance route → Skew → PLL, H-tree, reverse ..
- Toggle rate, data rate, DDR
- Transparency problems
- Meta-stability
- Gating
- Latch, FF, Register
- Static or Dynamic
- What else …

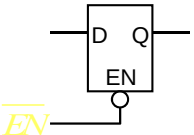
Latch

Function

1. Level-Enabled (E, EN, Enable, Clk)
2. Function: Q=D if E=1
   No Change if E=0

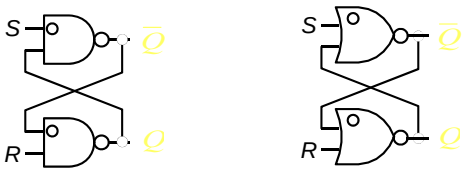


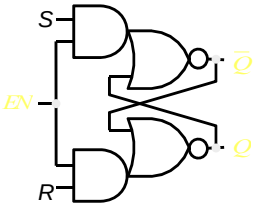
High-Level Enabled



Low-Level Enabled

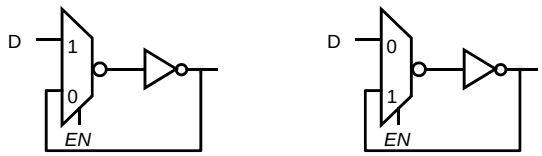
RS Latch



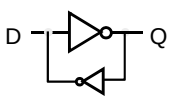


D Latch

Static:



Weak-Static:

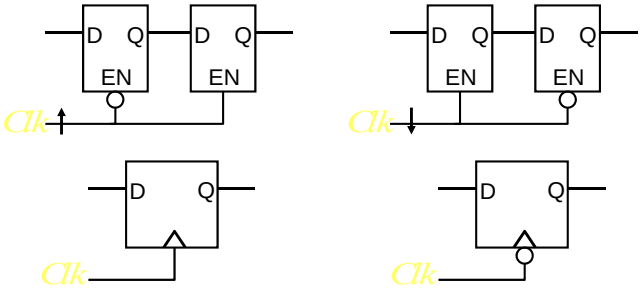


Dynamic:

Flip-Flops

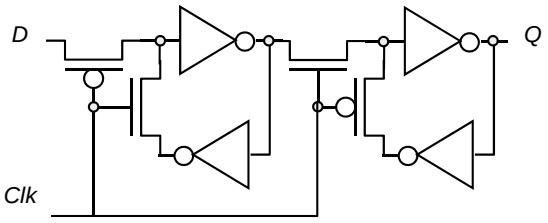
Function

1. **Edge-Triggered**
2. **Usually consisted of a low- and a high latches**

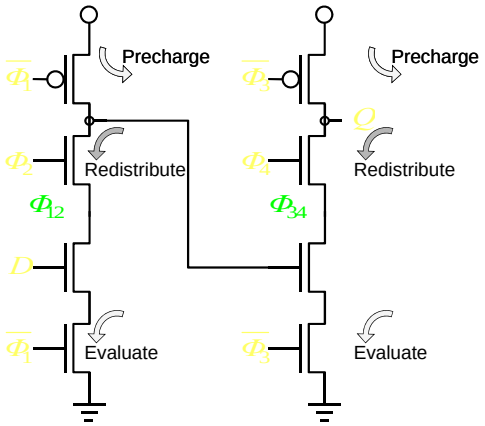


Flip-Flops

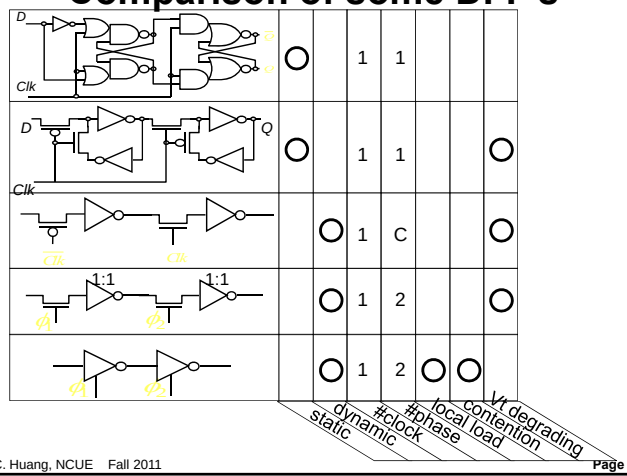
A small-area static positive-edge D Flip-flop *(Vdd>2Vt)*



4-Phase FF



Comparison of some DFF's

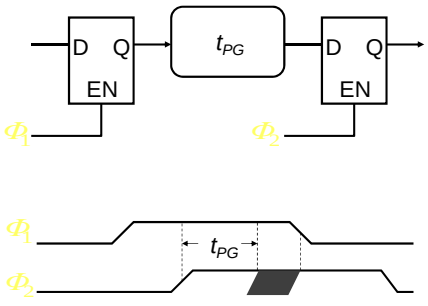


Synchronous v.s. Asynchronous Control

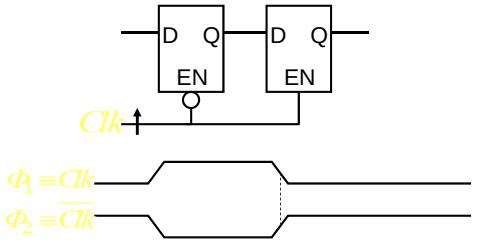
Settable, Resettable, etc.

	Synchronous	Asynchronous
Structural	Control, Q With Clk in the path to Q	Control, Q No Clk in the path to Q
Behavioral	always @(posedge Clk) if(Control) Controlled_state; else Clocked_circuit;	always @(posedge Clk or posedge Control) if(Control) Controlled_state; else Clocked_circuit;

Transparent Output



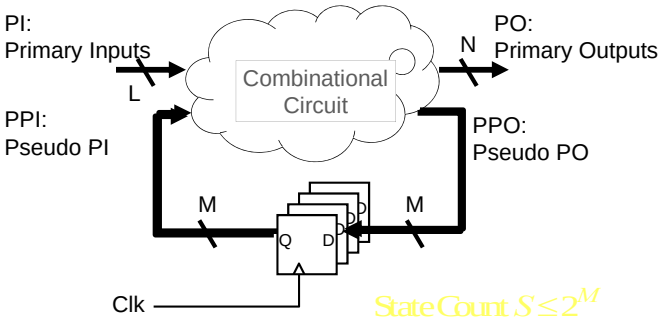
Flip-Flops without Transparency



Fully self-constrained!

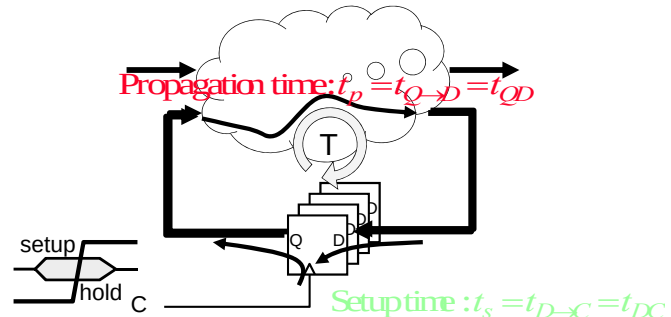
Clocking Strategies

Huffman Model for a Finite State Machine



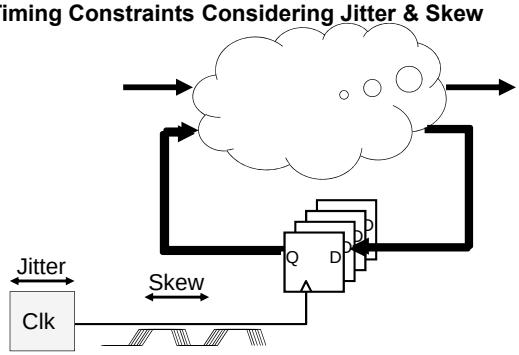
Clocking Strategies

Basic Loop Timing Constraints



Clocking Strategies

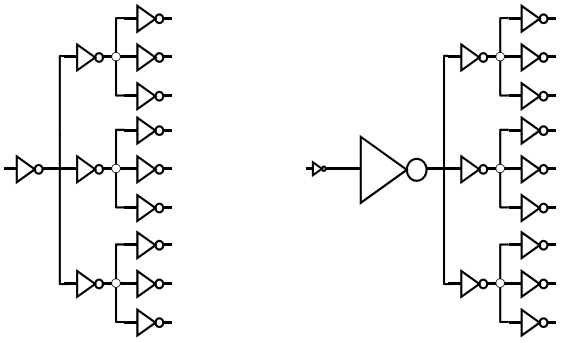
Timing Constraints Considering Jitter & Skew



Clock Buffering

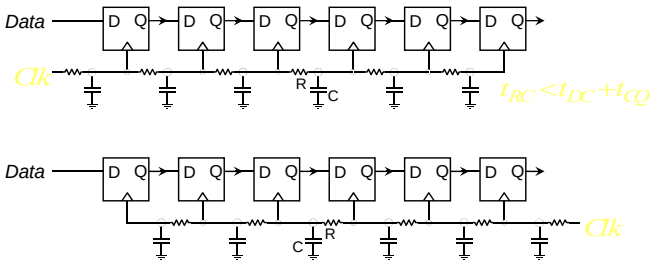
Clock Tree with a branch
Degree of 3 or 4 (~ 2.718)
without consideration of route

A single large buffer:



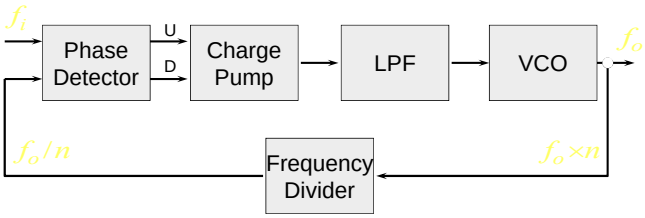
H-Tree

Contra-data Direction Clock



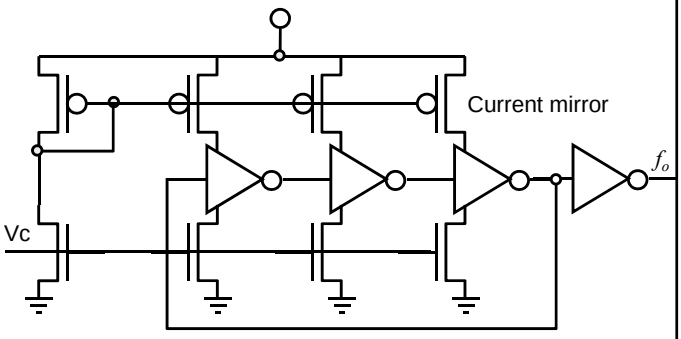
Generally, $T < nt_{RC} + t_{SK} + t_{DC} + t_{CQ} + t_{PG}$

Phase Lock Loop (PLL)



1. **Skew Reduction; Synchronization**
2. **Frequency Multiplier**
3. **Data Recovery**

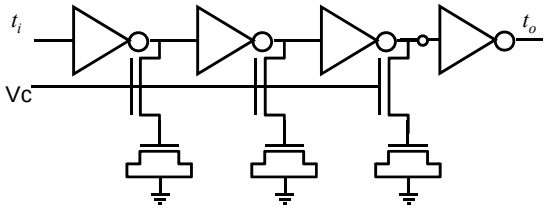
A Typical VCO



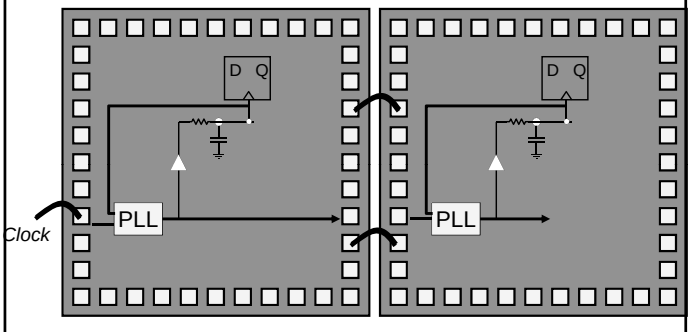
180-degree oscillator

VCDL

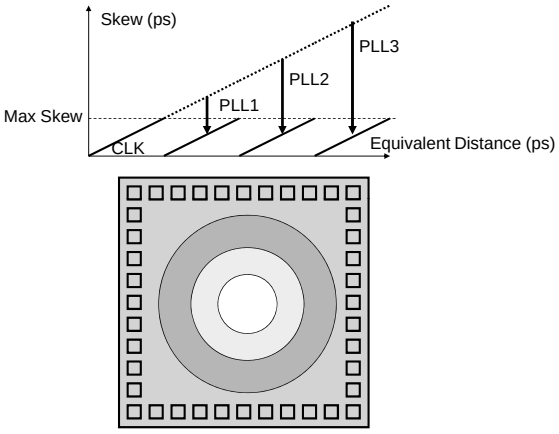
Voltage Control Delay Line



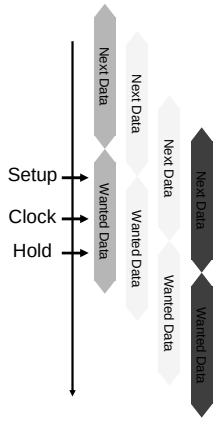
PLL Clock Generator

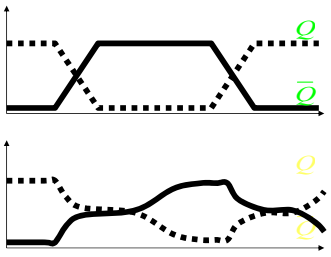


PLLs Applied to Different Domains



Metastability & Synchronization Failure



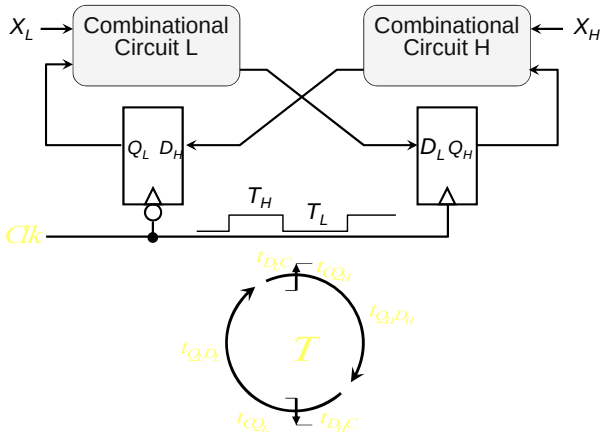


Logic Error!

Skew-Tolerant Design

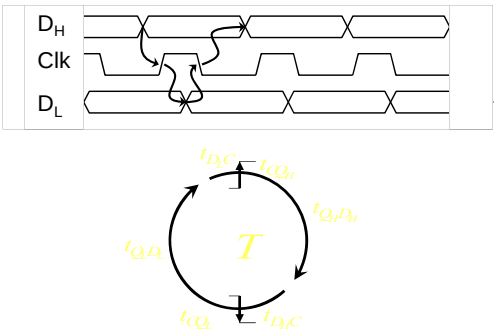
1. Reverse Order of Clocking for only scan
2. Skew-Tolerant Dynamic Circuit
3. Skew-Tolerant Domino
4. Clock Domain Ranging

Single-Clock Complementary Phase

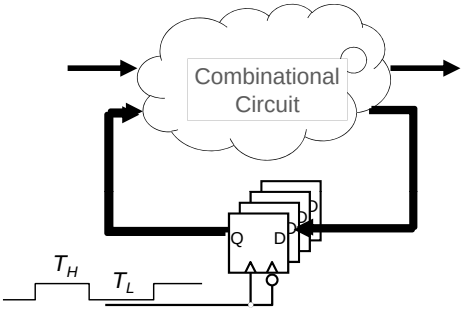


Single-Clock Complementary Phase

Timing Diagram

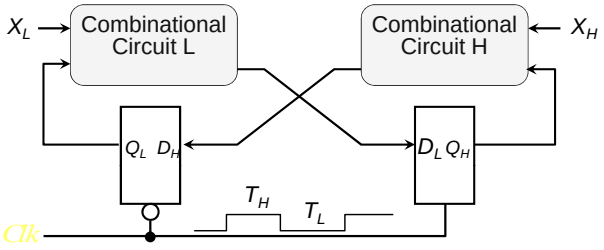


Single-Clock Double Edge



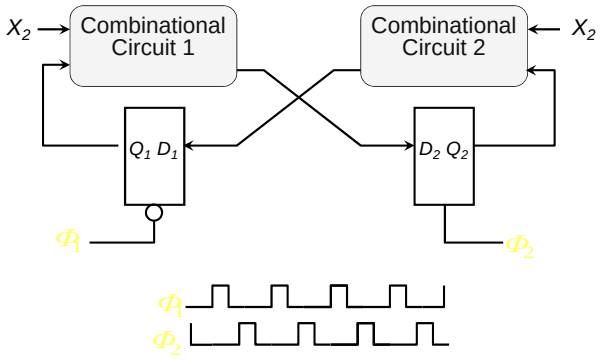
1. Can slack the master clock only.
2. $\frac{1}{f}=T_L+T_H;\ \min(T_L,T_H)>t_{CQ}+t_{QD}+t_{DC}+t_{H'}+t_{SK}$

Single-Clock Complementary Phase Latch System



Data Transparency!

Single-Clock 2 Phase

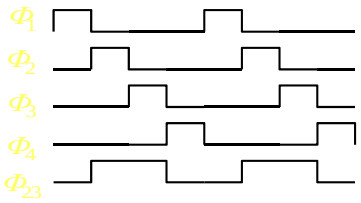


N-Phase Clock Notations

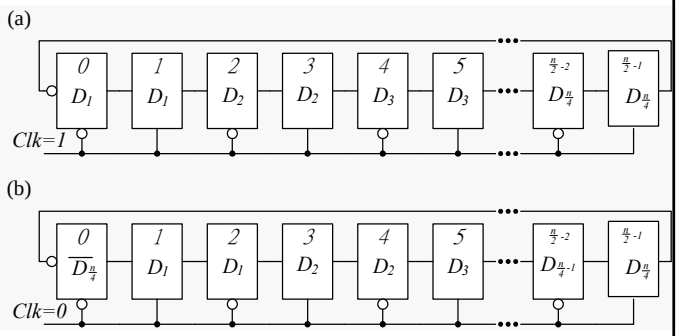
For convenience, a cycle is divided into N divisions.

$0 \cdots (N-1)$ or $1 \cdots N$

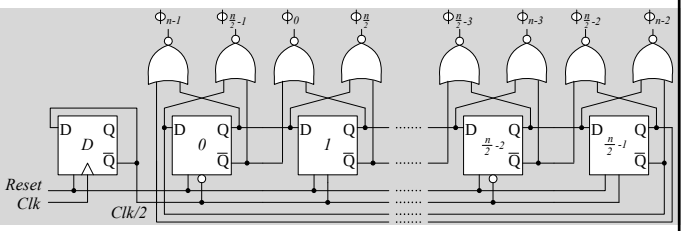
Φ_i denotes that it has a high level only in the ith division.



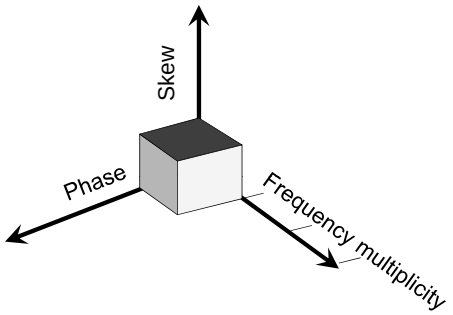
Johnson Counter



Multiple Phase Clock Generator



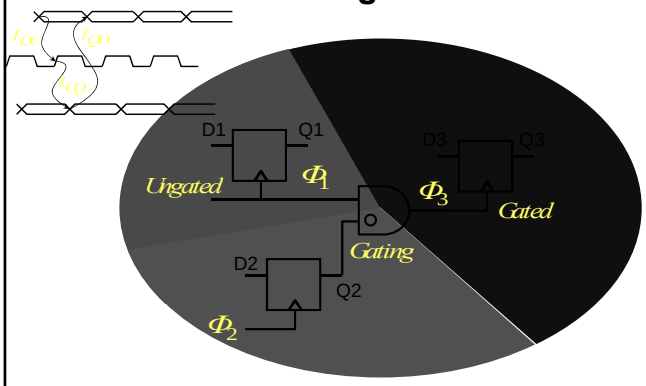
Clock Domain Programming



Clock Domain Interface

Leading Phase Logic	Latch-base Bufer	Lagging Phase Logic
Lagging Phase Logic	Latch-base Bufer	Leading Phase Logic with 1 cycle delay
Integer-Times Frequency	SIPO	Low--Frequency Circuit
Low-Frequency Circiut	PISO	Integer-Times Frequency
Skewed or Remote	PLL Data Recovery	Clock recovered But delayed

Clock Gating Problem



Discussed in advanced topic and should be careful!

A Simple Clock Gating Condition

1. **Single Clock, Single Phase, Positive-Edge Trigger for Ungated and Gated Circuits**
2. **Gating Signal can be synchronized at negative edges and generated from the complementary clock domain.**
3. **Assme Clock Gating delay: t_{CG}**

$$\frac{1}{f} = T > t_{CQ} + t_{QD} + t_{DC} + t_{JT} + t_{SK} + 2t_{CG}$$