國立彰化師範大學電子系 109 學年第二學期隨堂考考卷

課目：VLSI 設計導論 日期：2021/3/10(Wed.) 時間：08:30~09:00am 地點：E406 老師：黃宗柱

學號：_____ 姓名：_____ 得分：_____

Multiple Choice (單選題):

(O) 1. The unit of a sheet resistance is (A) H/cm^3, (B) Ω/cm, (C) Ω/cm^2, (D) Ω/cm^3.

(D) 2. Which resolution is the best in a typical process? (A) diffusion resistance, (B) polysilicon resistance, (C) M2-M3 capacitance, (D) frequency of a quartz oscillator.

(C) 3. How many 200-ps buffers are required for minimizing the delay of a 10-ns interconnection? (A) 4, (B) 5, (C) 6, (D) 7.

(A) 4. NAND g1(X, A, A); NOR g2(Y, B, B); XOR(Z, X, Y); are all CMOS gates. The chaacteristic curve of Z will be (A) _—_ (B) ⌙ (C) ⌜ (D) -_- .

(C) 5. In the saturation region of the IDS model of a CMOS transistor, IDS= (A) 0, (B) $\beta[(v_{GS}-V_{tn})v_{DS}-v_{DS}^2/2]$, (C)$\frac{\beta}{2}(v_{GS}-V_{tn})^2$, (D) $\frac{\beta}{2}(v_{DS}-V_{tn})^2$.

(C) 6. The output of a cascade of inverters with an input dc-slope < -1 will be (A) high, (B) low, (C) vanished, (D) oscillating.

(D) 7. Which dimension of a unitary CMOS inverter will be the largest? (A) Ln, (B) Lp, (C) Wn, (D) Wp.

(B) 8. Which range will be the largest? (A) coil inductance, (B) channel resistance, (C) metal condunctance, (D) diffusion resistance.

(A) 9. When the source of a NMOS is connected to the drain of another NMOS transistor, the substrate connected to GND is to prevent from (A) latchup effect, (B) stack effect, (C) body effect, (D) antenna effect.

(C) 10. When the source of a NMOS is connected to the drain of another NMOS transistor, the substrate connected to GND tends to result in the (A) latchup effect, (B) stack effect, (C) body effect, (D) antenna effect.

請公正評分，改卷者簽字：_____