VLSI Design

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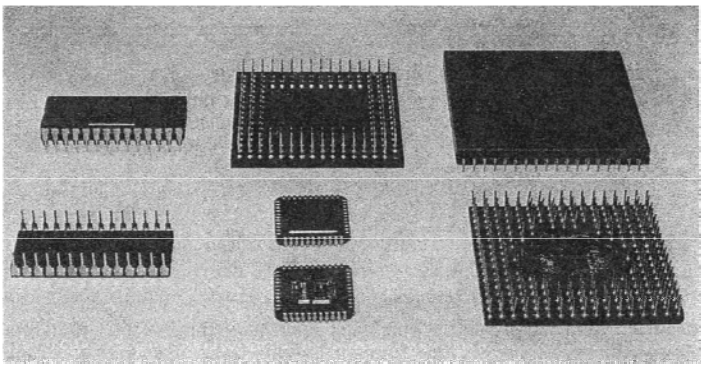
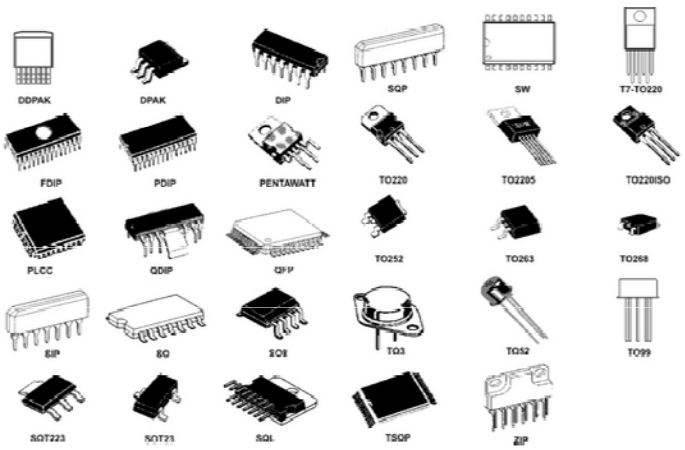
I/O Structures

1. **Bonding**
2. **ESD**
3. **I/O Pad**
4. **Power Pads**
5. **Guard Ring, Quiet Ring**
6. **Tristate and Bidirectional Pads**

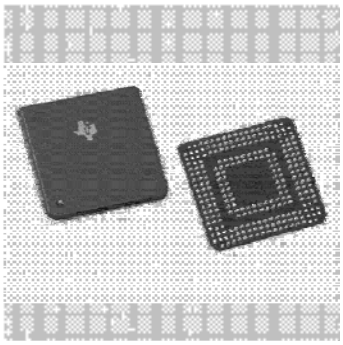
Packages



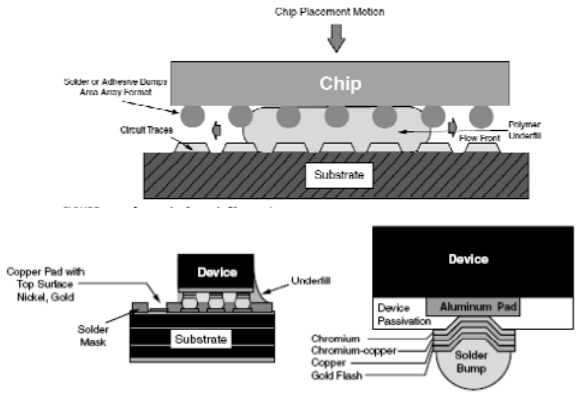
Packages



Ball-Grid Array (BGA)

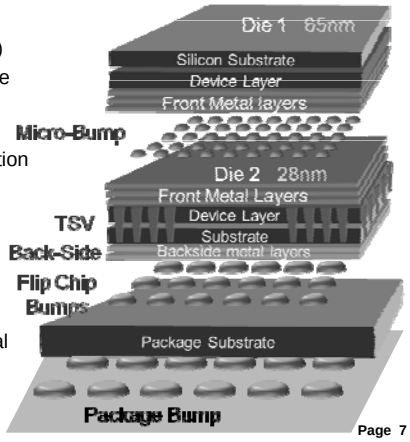


Bump and Trace

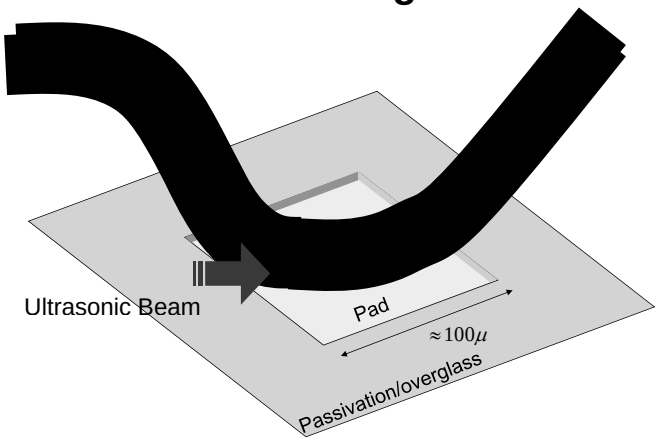


Examples of 3D-IC Stack

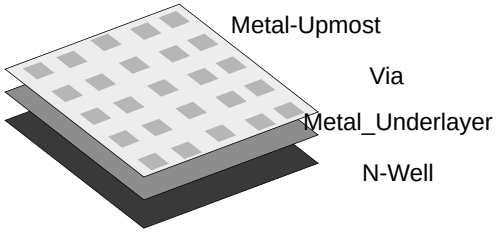
- 3D-IC stack modeling:
  - Stacking configuration (vertical, horizontal, mix)
  - M-bumps, TSV, backside metal, and flip chip
  - Multiple technologies
  - IC layer stack for extraction and thermal.
- 3D enabled Design implementation tools
- 3D floorplanning – bump optimization
- 3D analysis tools { R(L)C extraction, timing/SI, thermal and voltage drop.



Bonding



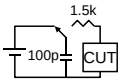
Pad Building



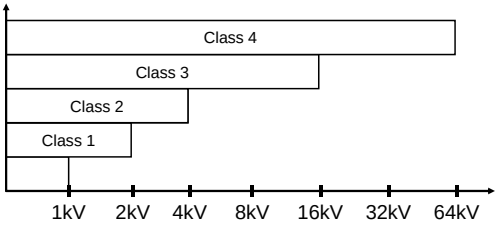
ESD

Electrostatic Discharge

1. **Usually, discharging time ~ 100ns**
2. **Input resistance ~ 1K for common ICs.**
3. **Test Bench:**

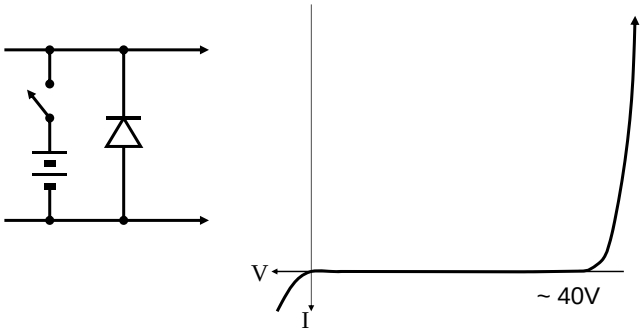


4. **ESD Classification:**

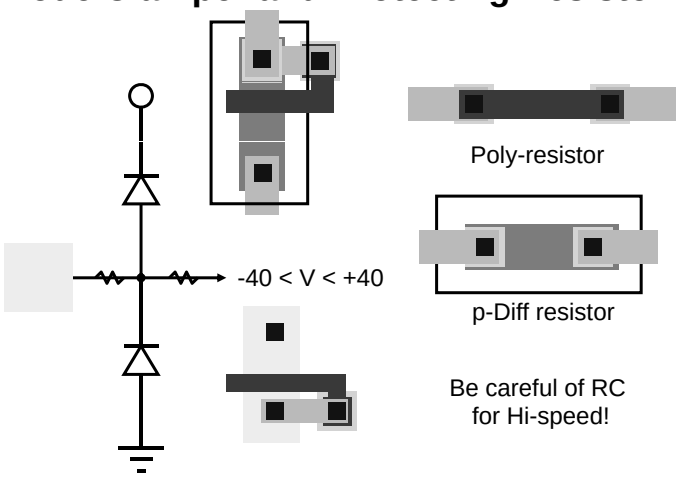


Thinox Puncture and Drain Breakdown

Typical ESD Protection

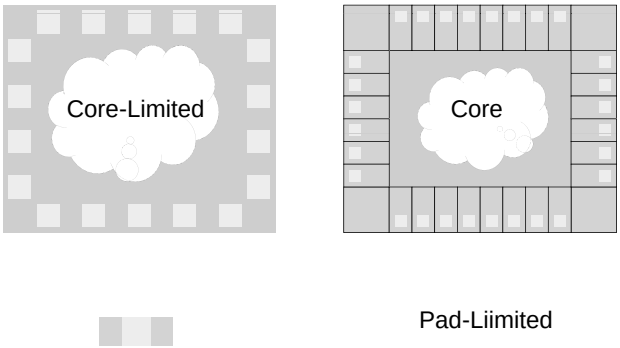


Diode Clamper and Protecting Resistor



Be careful of RC for Hi-speed!

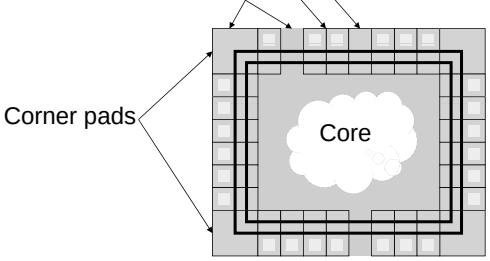
PAD vs. Core



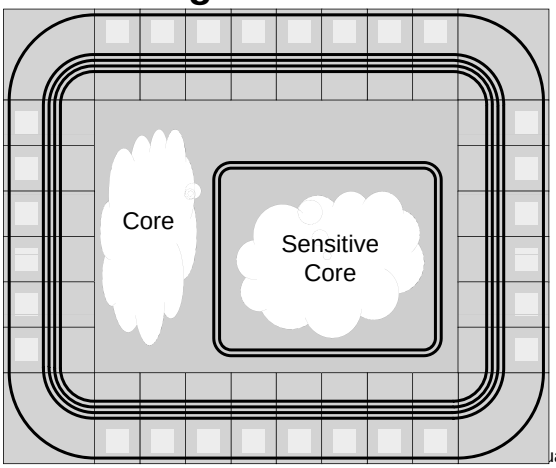
Pad-Liimited

Connection between PADs

1. **Butting**
2. **Feed-through**
3. **Wired**



Rings around the Cores



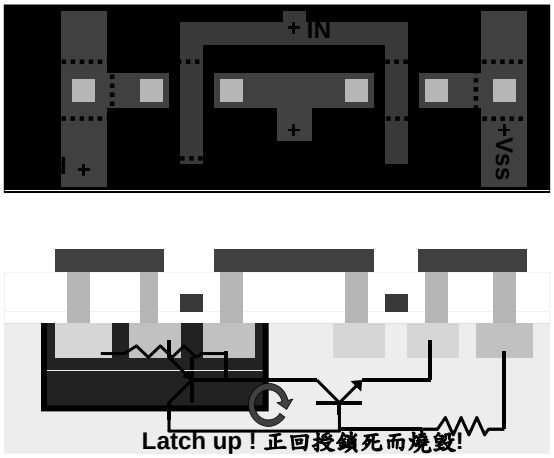
Guard Rings
Pad-Power Rings
Core-Power Rings
Quiet Rings
Dirty Rings
Clean Rings
Diffusion Rings
User Rings

ually lowest outer

Miscellaneous Pads

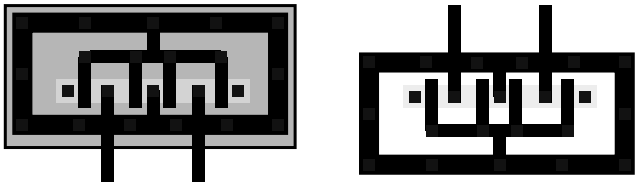
1. **Power Pads: Noise Prevention, Separation**
2. **Input Pads: Level-Shifting, Input Protection**
3. **Output Pads: Drive, Latch-up Prevention**
4. **Clock Pads: RC Reduction**
5. **Heat-sink Pads: (connected to) Heat Sink**
6. **Stand Pads: (e.g., LCD display)**
7. **Scan Pads: with Boundary Scan Cell**
8. **Virtual-Ground Pads: with SLEEP Transistor**
9. **Register Pads: to reduce t_{CQ}, t_{DC}**
10. **Schmitt-Trigger Pads**
11. **Pull-Up/Down Pads**
12. **Analog/Digital Pads**
13. **Dirty/Clean Pads**

Latch-up Effect in n-Well Process

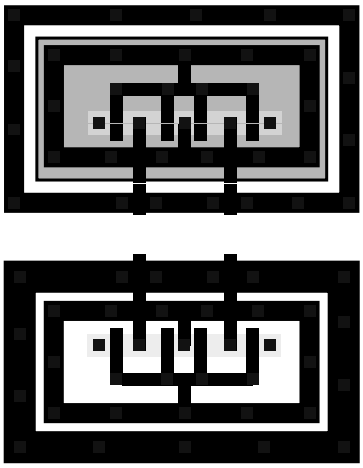


Guard Rings

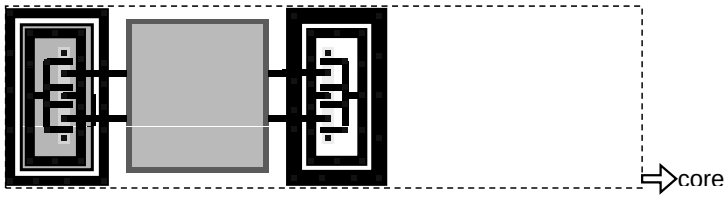
1. **Noise Reduction**
2. **Latch-up prevention especially for Output (Hi-I) Pads**
3. **To guard deeply (under thinox), Diffusion Rings are usually used.**
4. **For diffusion rings, Poly-crossovers are inhibited.**



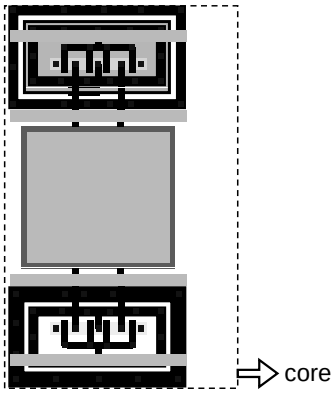
Doubly Guard Rings



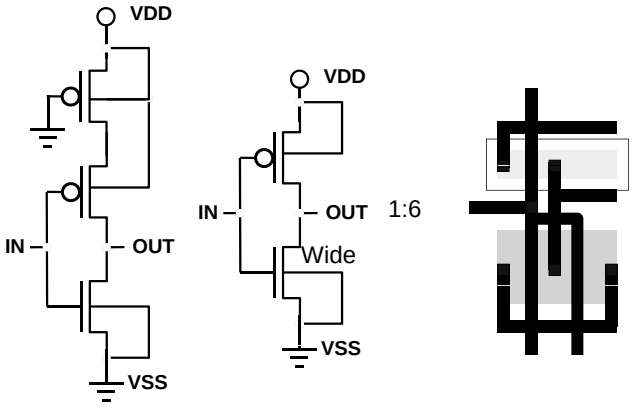
Pad-Limited Pads



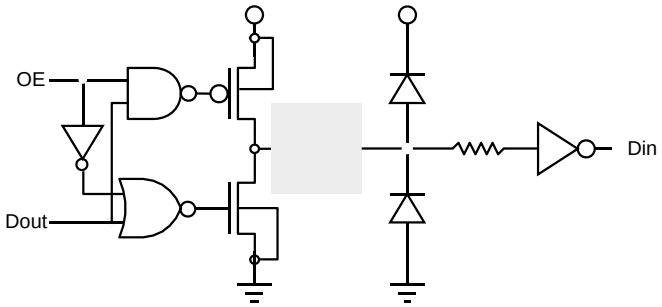
Core-Limited Pads



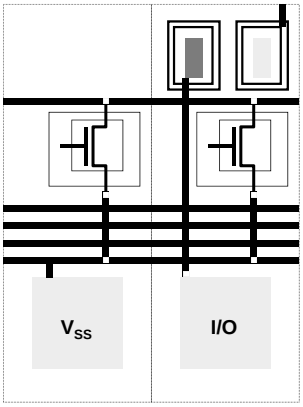
TTL Input PAD



A Tri-state/Bidirectional Pad



Sleep Transistor in Pads



Boundary Scan Cell in I/O Pad