

Final Examination Sheet

Spring Semester, 2021, Dept. of Electronics Eng., National Changhua Univ. of Edu.

Course : **Introduction to VLSI Design** Date : 2021/6/23 (Wed.) Time : 09:20~11:00 Online Exam.

Note: You can answer your exam by one of the following steps:

1. Please full-in or paste your answer by drafting using PowerPoint or Excel, transfer to pdf, name the file using your Reg.No and email to tch@cc.ncue.edu.tw by 11:20am.
2. Otherwise, you can write down your answers on paper and have a picture by camera, (paste them to a winword file, transfer to pdf), name the file using your Reg.No, and then email to tch@cc.ncue.edu.tw.

Reg. No. : _____

Student's Name : _____

I. TRUE OR FALSE (Mark \bigcirc or \times , 20%):

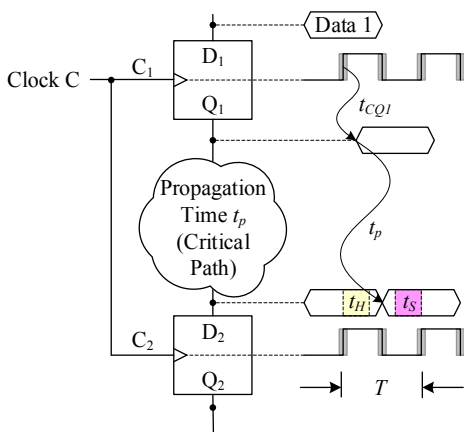
- () 1. SKILL is a scripting language which can be applied in Virtuoso for full-custom layout.
- () 2. "module m(C, I, O); input C, I; reg O; always@(posedge C) O=I; endmodule" can be correctly compiled in Verilog.
- () 3. An 8-bit adder is verified if the output is 20 for inputs 13 and 7.
- () 4. It is called technology mapping to implement Boolean functions into specific logic cells.
- () 5. EDA Scripting is to take ≥ 1 general or tool command language interpreters to automate ≥ 1 electronic design packages.
- () 6. The rule of tens approximately explains the decision whether to test or not in each manufacturing stages.
- () 7. Usually a 16GB NOR type Flash SD is more expensive than the a 32GB NAND type Flash memory stick.
- () 8. The increment c++ in C language takes about one half of gate count and one half of carry propagation time.
- () 9. 0-1 march test $\uparrow w0 \uparrow r0 \uparrow w1 \uparrow r1$ detects more faults than $\uparrow w0r0 \uparrow w1r1$.
- () 10. IC test can be fully saved if a fault tolerant mechanism is built in.

II. MULTIPLE CHOICE (Choose the best one, 20%):

- () 1. Which is not a purpose of growing poly-silicon prior to iron implementation, (A) serving as a mask (B) preventing from latchup (C) working as a transistor gate (D) self-alignment.
- () 2. In a high-voltage layout which is usually enhanced? (A) thinox thickness (B) gate extension (C) transistor pitch (D) drain distance.
- () 3. A recent global problem is the shortage of (A) water (B) automotive chips (C) labor (D) capital.
- () 4. Which control signal provides a short and constant-width pulse? (A) Reset (B) Clock (C) Toggle (D) Strobe.
- () 5. Which type of logic structure usually takes low power and long time? (A) AOI (B) OAI (C) NOR (D) NAND.
- () 6. Which diagram shows the working boundaries of products? (A) I-V (B) Space-Time (C) Shmoo (D) ladder diagram.
- () 7. Which is mainly responsible for transistor-level simulation? (A) Encounter (B) Debussy (C) HSPICE (D) Virtuoso.
- () 8. Owing to clock wire resistance, shift registers overpass in a cycle is caused by (A) transparent output (B) setup time violation (C) hold time violation (D) bus contention.
- () 9. Voltage-dividing effect of an SRAM cell tends to occur at its (A) write (B) standby (C) read (D) search mode.
- () 10. Which adder is usually designed for many inputs? (A) carry skip (B) carry select (C) carry save (D) carry ripple.

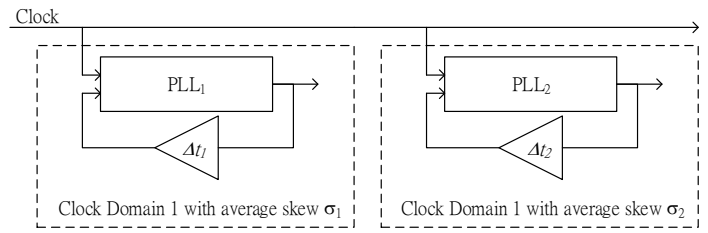
III. QUESTIONS (120%, at most 60% adopted):

1. As the following figure, the peak-to-peak jitter and skew is defined as the maximum $t_{CIC2} = t_J$. Clock-to-Q times t_{CQ} of successive flip-flops FF1 and FF2 are given. The critical path of the combinational circuit takes a t_p propagation time. Hold time t_H and setup time t_S are constraint constant time for flip-flops. Derive the setup-time and hold-time rules in two inequations according to the following figure. (20%)

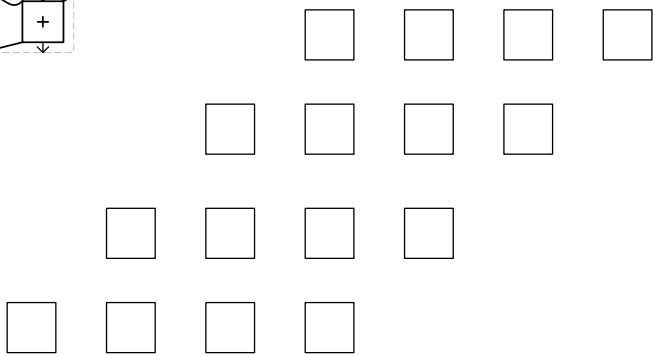
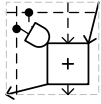


2. Draw a typical diagram of a RAM array according to the lecture. (15%) (including row/col address decoders, SA, WLs, BLs, controller, SRAM cells, etc.)

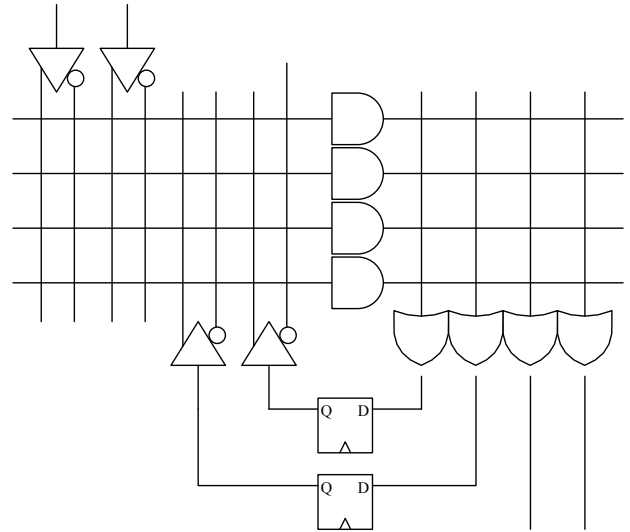
3. In the following figure, PLL_i means the i -th ideal phase lock loop to provide clock source of domain i with an average skew σ_i . To reduce the relative skew of all domains, a delay line with delay Δt_i is applied to feed back loop. Explain the operations and calculate the relation between Δt_i and domain average skews. (15%)



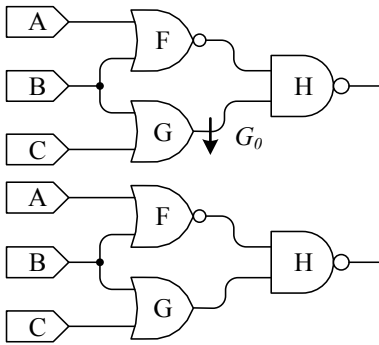
4. A multiplier cell is given. Draw a 4×4 parallel multiplier with 4×4 cells. The input/output paths drawn in dashed lines and the carry paths solid lines. (15%)



5. Using a typical FSM design procedure, design a 1-input 1-output sequence detector that will outputs 1 only when it receives a sequence 1111. Implement the FSM by programming (burn on with a notation X) on the following PLA diagram (with AND and OR arrays). (20%)



6. Given the fault list of the following circuit as $L_f = \{A_0, A_1, B_0, B_1, C_0, C_1, F_0, F_1, G_0, G_1, H_0, H_1\}$ where G_x means gate G stuck-at-x fault, (1) justify and propagate to find the test pattern T_{G_0} of G_0 . (2) Then do deductive fault simulation to collect all testable faults of T_{G_0} . (3) Calculate the fault coverage of T_{G_0} , $FC(T_{G_0}, L_f)$. (20%)



7. Assume F is a 3-input function, $F = A\bar{B} + B\bar{C}$, map and program F into the following different structures. Write the bitstream for programming the LUT. (15%)

