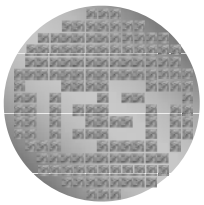

VLSI Design

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2016/05/03

Clocking Strategies

1. Clocked System
2. Latch and Registers
3. System Timing (Constraint)
4. Single-Phase Memory
5. Phase Locked Loop Clock Techniques
6. Metastability and Synchronization Failure
7. Single-Phase Logic Structure
8. Two-Phase Clocking
9. Two-Phase Memory Structure
10. Two-Phase Logic Structures
11. Four-Phase Clocking
12. Four-Phase Memory Structures
13. Four-Phase Logic Structures
14. Clock Distribution

Clocking Strategies

Clocked System

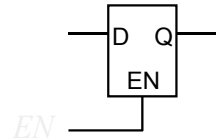
Considerations:

- Independent Clock Count
- Clock phase count for each independent clock
- Clock domains
- Synchronous or Asynchronous
- Clock-Generator: Jitter
- Distance route → Skew → PLL, H-tree, reverse ..
- Toggle rate, data rate, DDR
- Transparency problems
- Meta-stability
- Gating
- Latch, FF, Register
- Static or Dynamic
- What else …

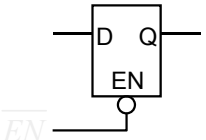
Latch

Function

1. Level-Enabled (E, EN, Enable, Clk)
2. Function: Q=D if E=1
   No Change if E=0

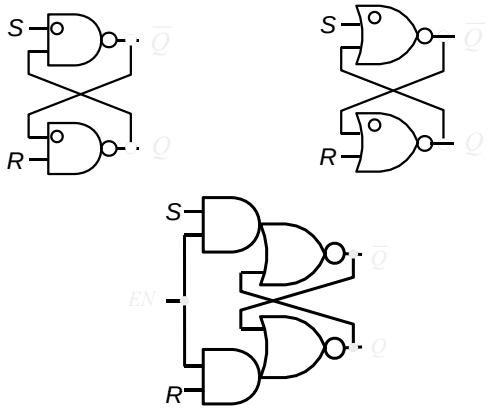


High-Level Enabled



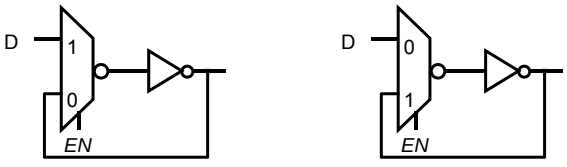
Low-Level Enabled

RS Latch

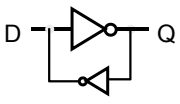


D Latch

Static:



Weak-Static:

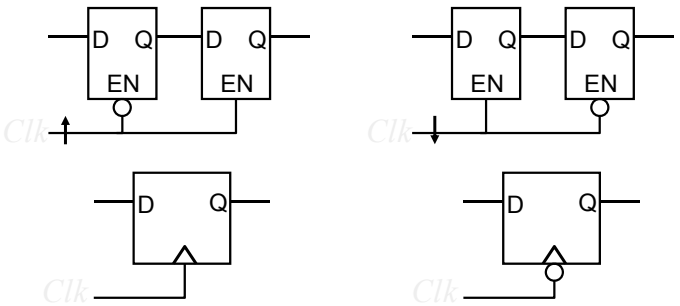


Dynamic:

Flip-Flops

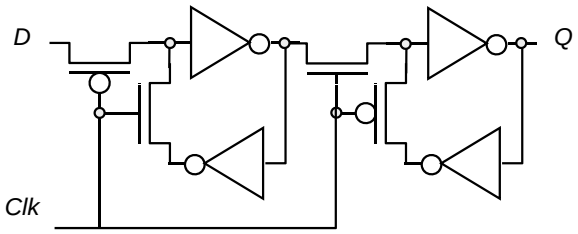
Function

1. **Edge-Triggered**
2. **Usually consisted of a low- and a high latches**

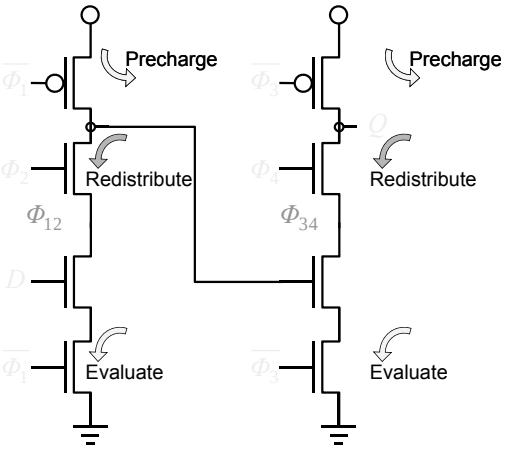


Flip-Flops

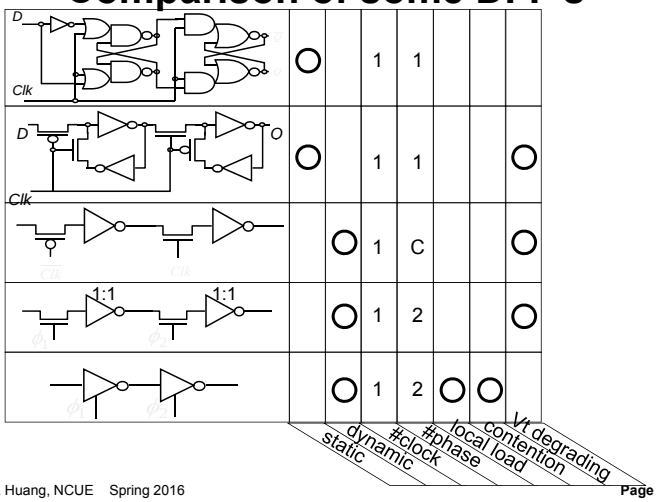
A small-area static positive-edge D Flip-flop *(Vdd>2Vt)*



4-Phase FF

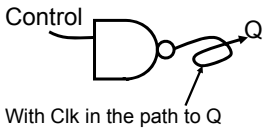
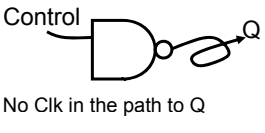


Comparison of some DFF's

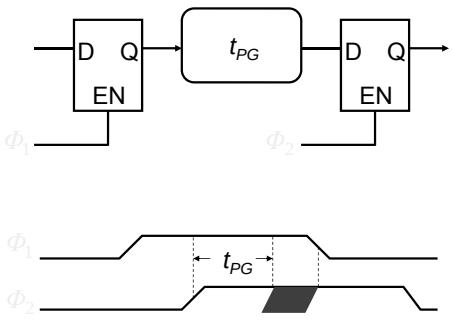


Synchronous v.s. Asynchronous Control

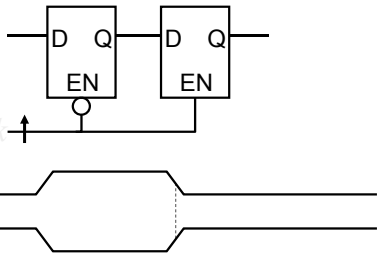
Settable, Resettable, etc.

	Synchronous	Asynchronous
Structural	 With Clk in the path to Q	 No Clk in the path to Q
Behavioral	always @(posedge Clk) if(Control) Controlled_state; else Clocked_circuit;	always @(posedge Clk or posedge Control) if(Control) Controlled_state; else Clocked_circuit;

Transparent Output



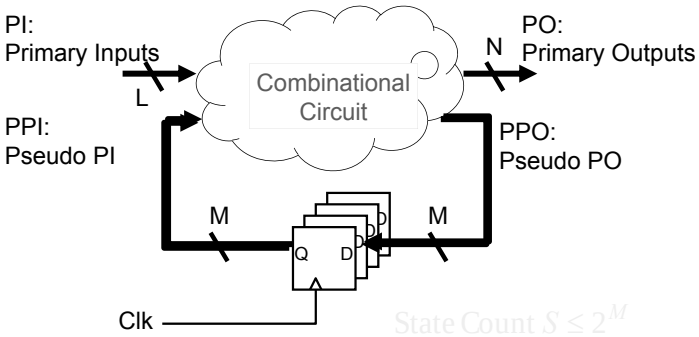
Flip-Flops without Transparency



Fully self-constrained!

Clocking Strategies

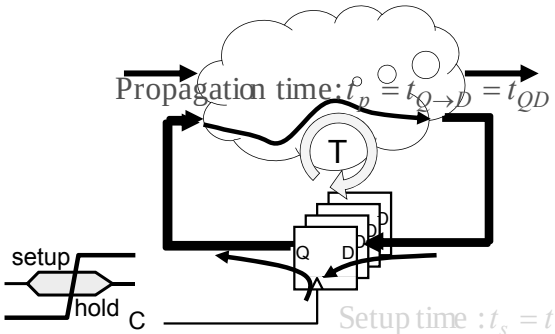
Huffman Model for a Finite State Machine



State Count $S \le 2^M$

Clocking Strategies

Basic Loop Timing Constraints



Propagation time: $t_p = t_{Q \to D} = t_{QD}$

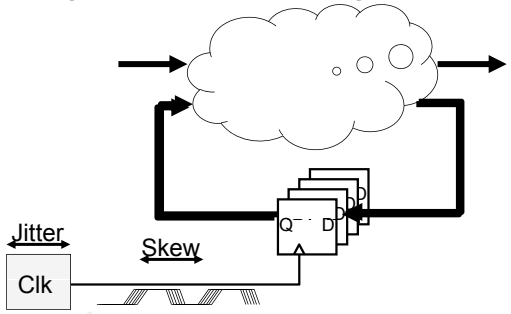
Setup time : $t_s = t_{D \to C} = t_{DC}$

Clock-to-Q time: $t_{C \to Q} = t_{CQ}$

Cycle time : $\frac{1}{f} = T > t_{CQ} + t_{QD} + t_{DC}$

Clocking Strategies

Timing Constraints Considering Jitter & Skew

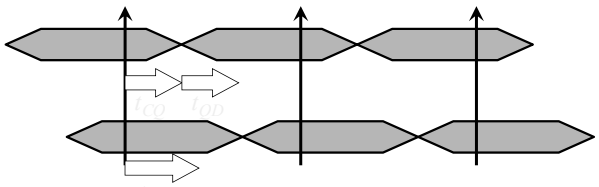


$\frac{1}{f} = T > t_{CQ} + t_{QD} + t_{DC} + t_{JT} + t_{SK}$

Setup-time violation : $t_{DC} = T - (t_{CQ} + t_{QD} + t_{JT} + t_{SK}) < t_{setup}$

Clocking Strategies

Hold-time Violations

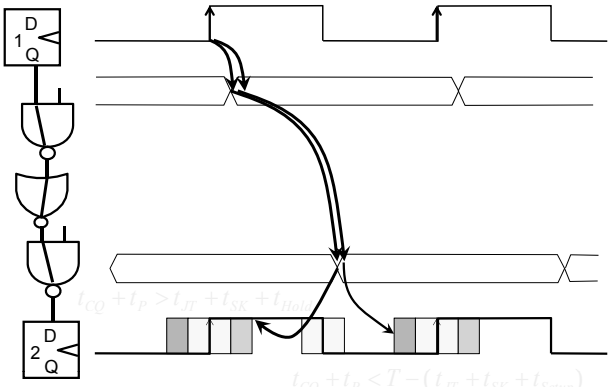


$t_{CQ} + t_{QD} \pm t_{JT} \pm t_{SK} > t_{hold}$

Hold-time violation : $t_{CQ} + t_{QD} < t_{hold} + t_{JT} + t_{SK}$

Clocking Strategies

Hold-Time Rule & Set-Time Rule

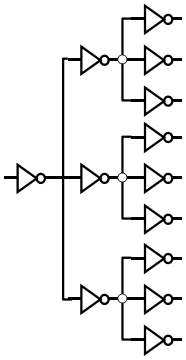


$t_{CQ} + t_p > t_{JT} + t_{SK} + t_{hold}$

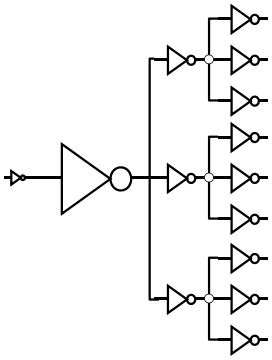
$t_{CQ} + t_p < T - (t_{JT} + t_{SK} + t_{setup})$

Clock Buffering

Clock Tree with a branch
Degree of 3 or 4 (~ 2.718)
without consideration of route

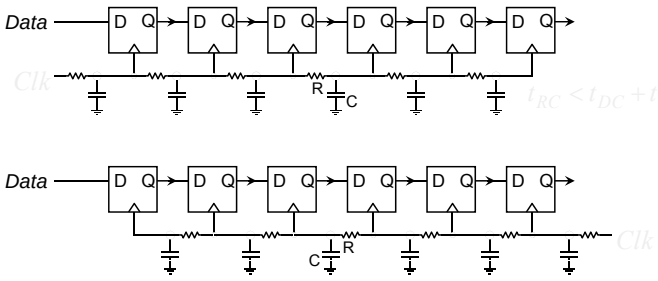


A single large buffer:



H-Tree

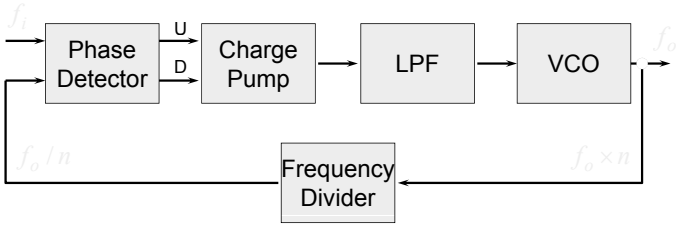
Contra-data Direction Clock



$t_{RC} < t_{DC} + t_{CQ}$

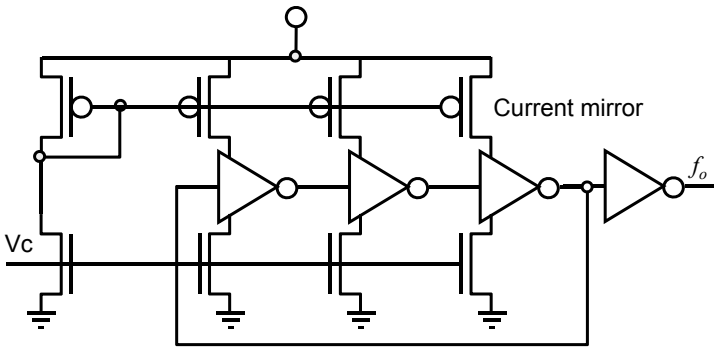
Generally, $T < nt_{RC} + t_{SK} + t_{DC} + t_{CQ} + t_{PG}$

Phase Lock Loop (PLL)



1. **Skew Reduction; Synchronization**
2. **Frequency Multiplier**
3. **Data Recovery**

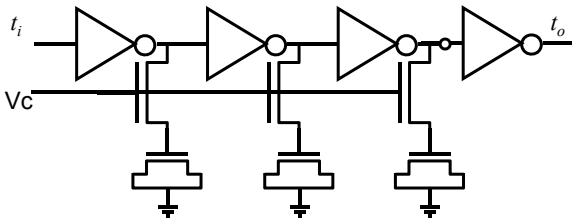
A Typical VCO



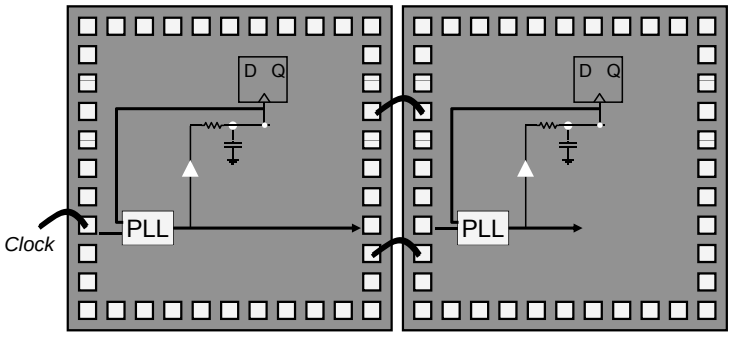
180-degree oscillator

VCDL

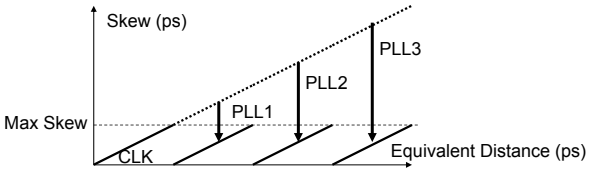
Voltage Control Delay Line

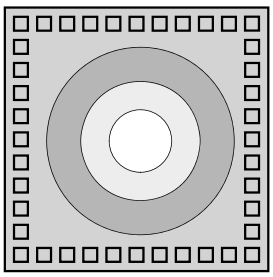


PLL Clock Generator

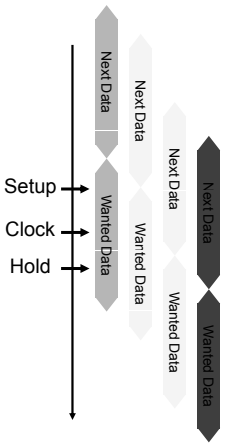


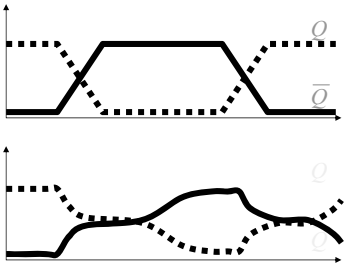
PLLs Applied to Different Domains





Metastability & Synchronization Failure



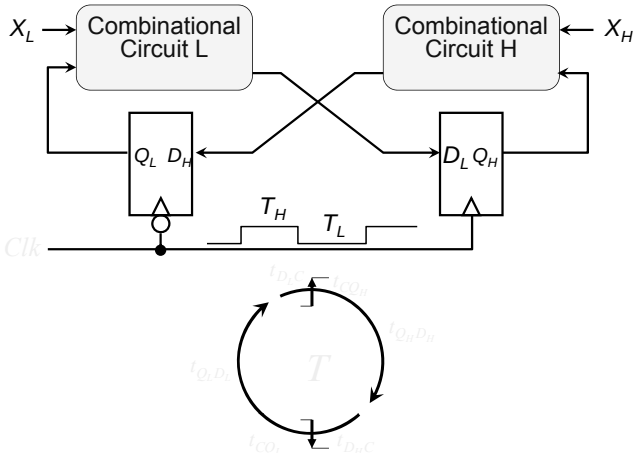


Logic Error!

Skew-Tolerant Design

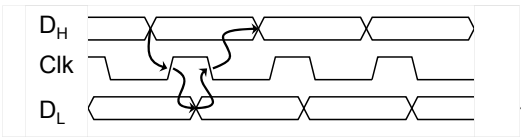
1. **Reverse Order of Clocking for only scan**
2. **Skew-Tolerant Dynamic Circuit**
3. **Skew-Tolerant Domino**
4. **Clock Domain Ranging**

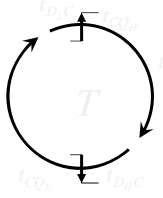
Single-Clock Complementary Phase



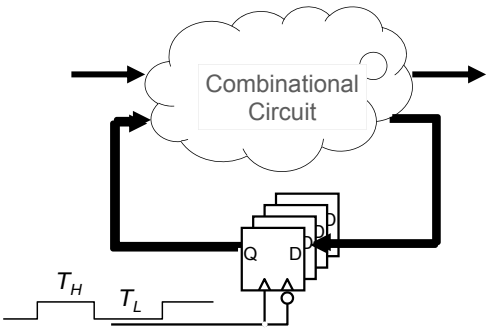
Single-Clock Complementary Phase

Timing Diagram



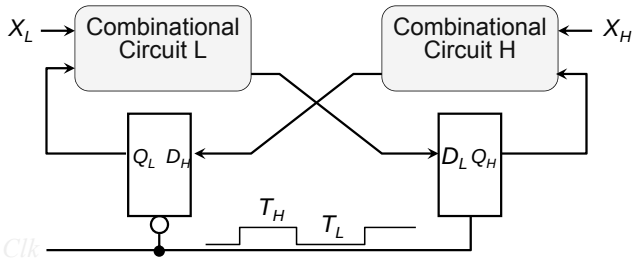


Single-Clock Double Edge



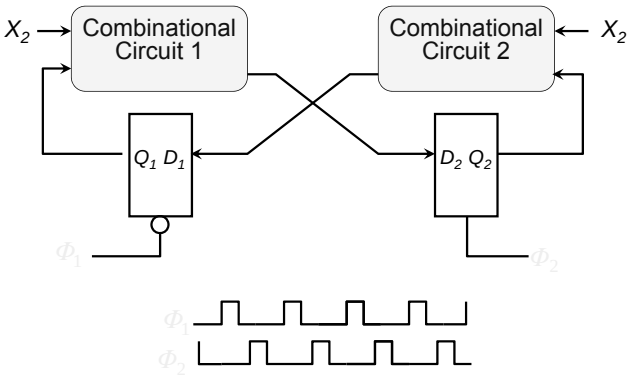
1. **Can slack the master clock only.**
2. $\frac{1}{f} = T_L + T_H;\ \min(T_L, T_H) > t_{CQ} + t_{QD} + t_{DC} + t_{JT} + t_{SK}$

Single-Clock Complementary Phase Latch System



Data Transparency!

Single-Clock 2 Phase

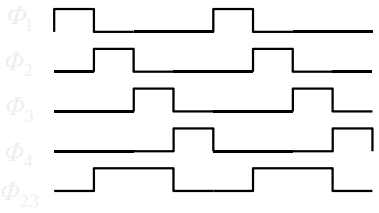


N-Phase Clock Notations

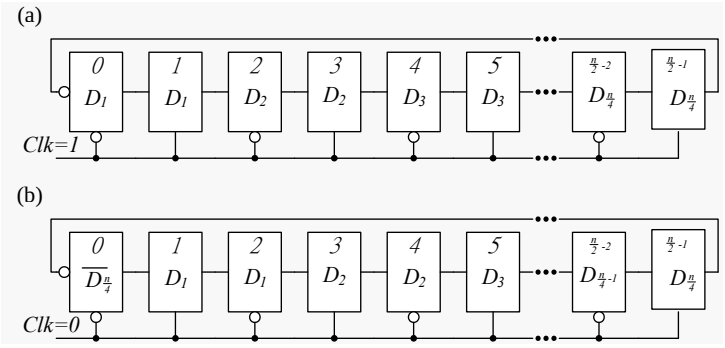
For convenience, a cycle is divided into N divisions.

$0 \cdots (N-1)$ or $1 \cdots N$

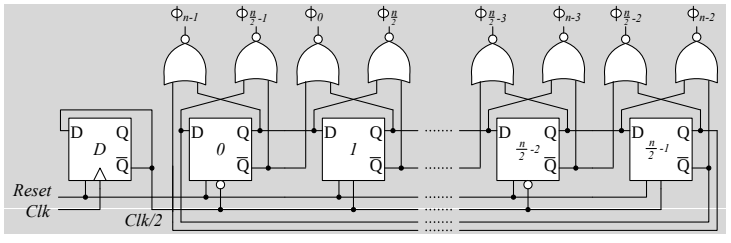
Φ_i denotes that it has a high level only in the ith division.



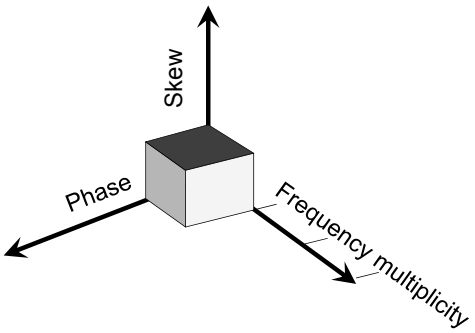
Johnson Counter



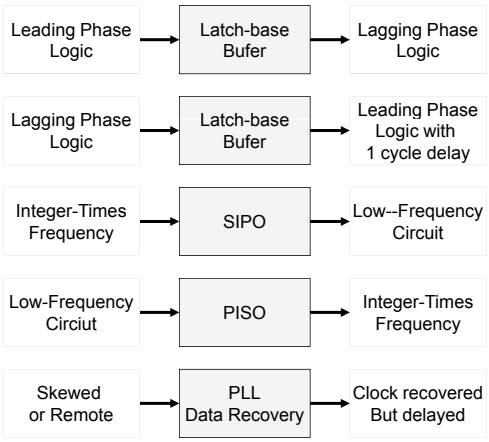
Multiple Phase Clock Generator



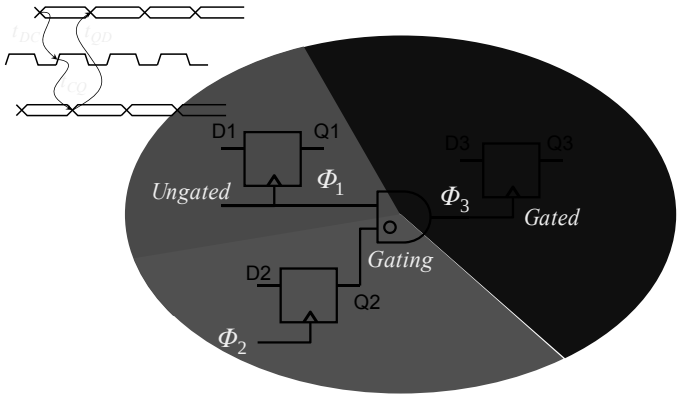
Clock Domain Programming



Clock Domain Interface



Clock Gating Problem

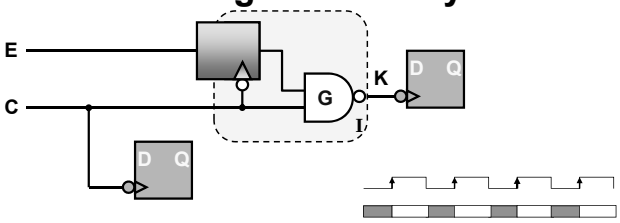


Discussed in advanced topic and should be careful!

Design Guide for Clock Gating

- Traditional Rules
  - ✓ Avoid from tri-state buffer and clock gating
- Later Moderate Rules
  1. Prevent from inverting polarity, i.e., use non-inversion gating.
  2. Control values should be glitch-free during high (low)-level clock pulse for positive (negative)-edge triggered flipflops.
  3. The control logic can have glitches/hazards only when the clock level can control them.
  4. Usually, the control logic is triggered by negative (positive) edge of the same clock for gating positive (negative)-triggered flipflops.
  5. Prevent from using tri-state gating along the clock paths.

Clock-Gating Cells for Synthesis

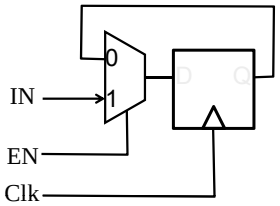


Label	Signal	0	1	Rule
C	Regular Clock	↓	↑	I = C⊕K
I	Inversion Type	Non-inverted	Inverted	
K	Gated Clock	↓	↑	
L	Latch Type	Low-level	High-level	L = ~C
G	Gate Type	OR	AND	G = E
E	Enable/Disable	Disable	Enable	

DFF2REG Design

- Comparison
  - ✓ DFF changes by all triggering clock events.
  - ✓ REG changes by its enabling commands only.
- Implementation
  - ✓ Multiplexed Control: + Level-Enable. - Area Overhead
  - ✓ Gated Clock: + Multiplexer Saving. - Skew Issue

(1) Level-Enable Distribution



(2) Gated-Clock Distribution