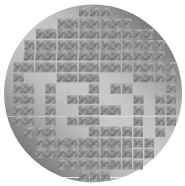

VLSI Design

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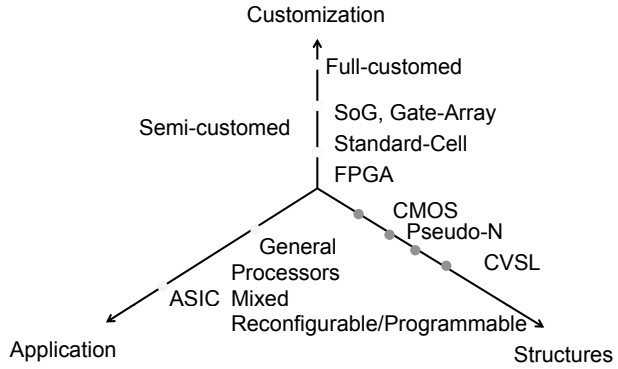
2016/03/29

Types of Logic ICs



Transistor-Level Structure
Outline

1. **CMOS Logic Gate Design**
2. **Standard Cell Layout & Channel Routing**
3. **Gate Array Layout**
4. **Sea of Gates**
5. **CMOS Layout Guideline**
6. **Transmission Gate Layout**
7. **MUX Layout**
8. **Pass-Transistor Logic**

Transistor-Level Structure
Outline

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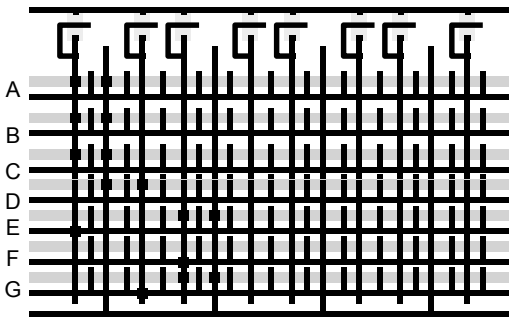
8. **Pass-Transistor Logic**

Rapid Prototyping

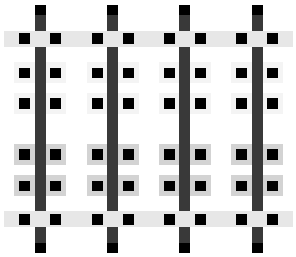
1. Prototyping: $Q << Q_{product}$ for test, debug, verification.
2. Rapid Prototyping: $t(Q) << t(Q_{product})$
3. Usual Rapid Prototyping wrt. Full Custom
   - Semi-Custom: saving the prior processes
     - Weinberger Array, Gate Array, SOG, e.t.c.
   - Standard-Cell: saving
   - PLD
     1) SPLD
     2) CPLD
     3) FPGA

Weinberger Array (NOR Logic)

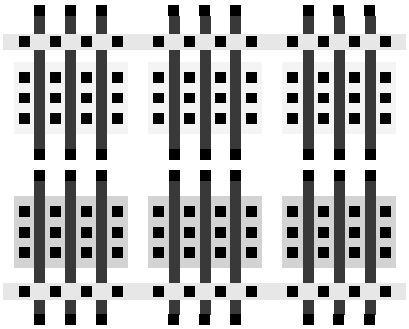


$F = (A + B + C)D$ $\quad Out = \overline{A + B + C + D}$

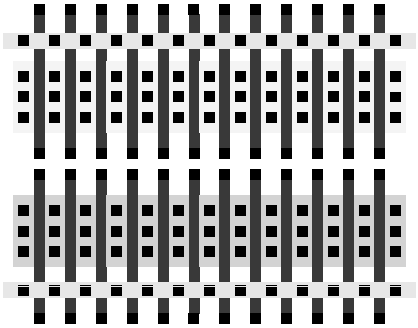
Gate Matrix



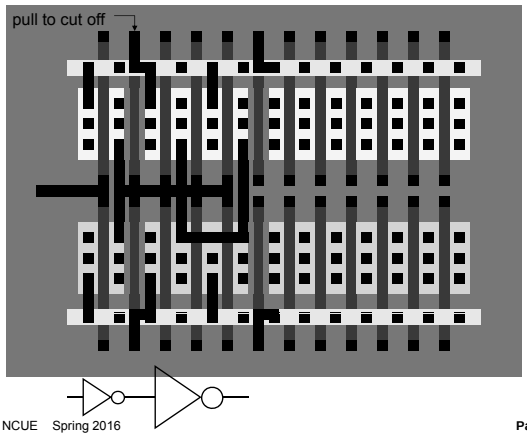
Gate Array



SOG: Sea-of-Gates

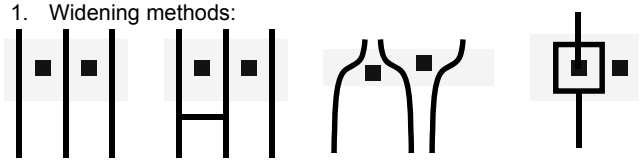


Example of SOG Design

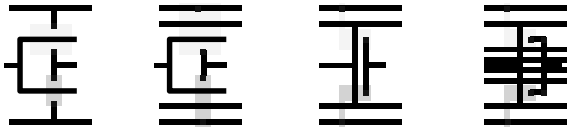


Physical Layout Skills

1. Widening methods:

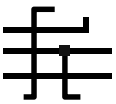


2. Crossover:

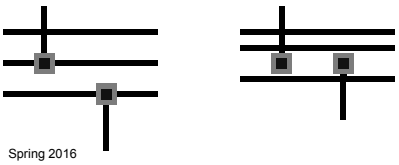


Physical Layout Skills

3. Dog-bone/Dog-Leg: No need to change layers for crossing

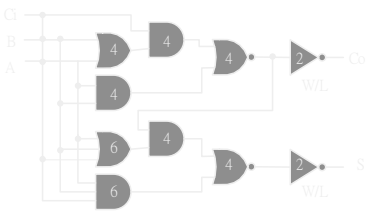


4. More usage of white space: Rubber forcing



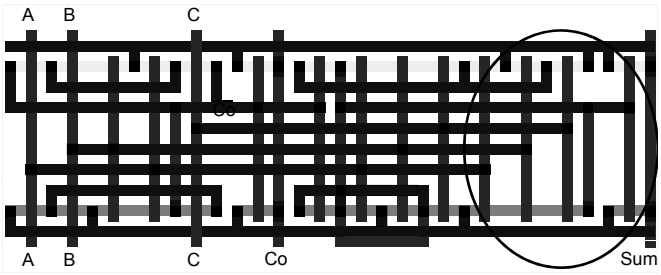
Folding Lines of Diffusion

Example: Full Adder



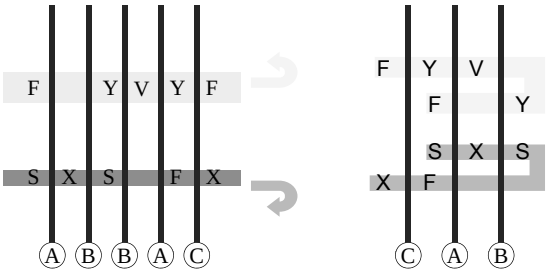
Folding Lines of Diffusion

Example: Full Adder



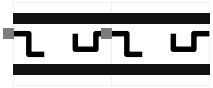
Folding Lines of Diffusion

Example: Sum=A⊕B⊕C

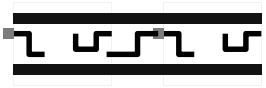


Connections of Standard Cells

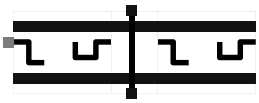
1. Butting



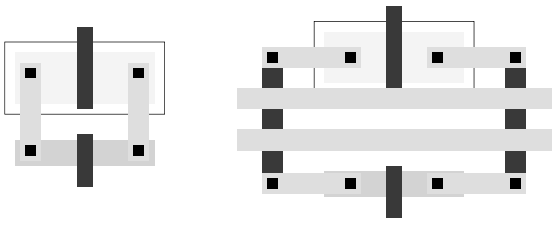
1. Wired



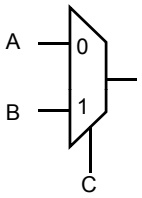
3. Feedthrough

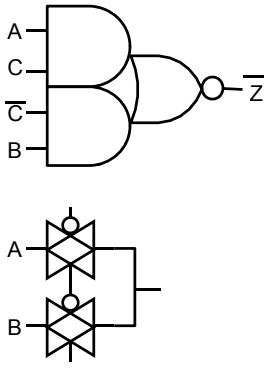


Transmission Gate Layout Consideration

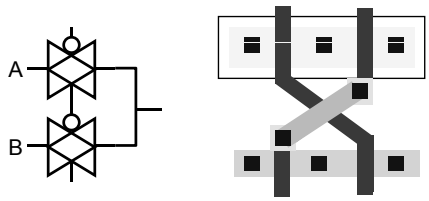


Multiplex

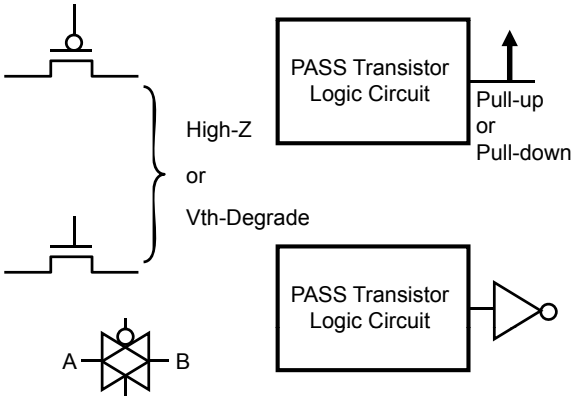




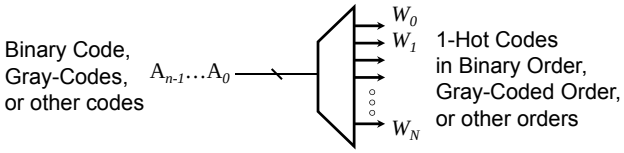
Multiplex Layout



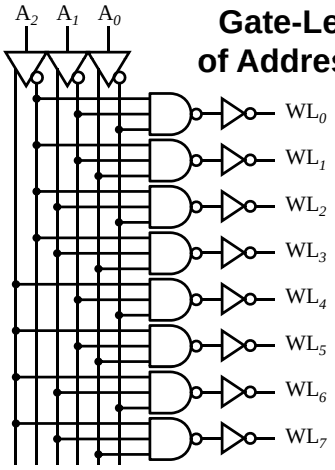
Pass-Transistor and Transmission Gate



Function of *n-to-N* Address Decoders

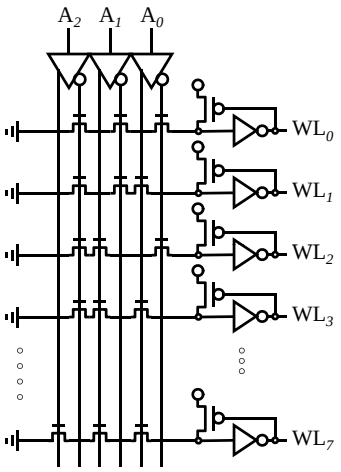


Gate-Level Design of Address Decoders

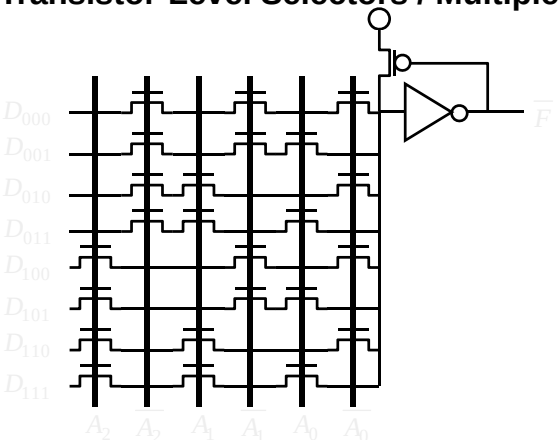


- The NAND can be substituted by NOR gates
- The gates can be CMOS cells in cell-based design, or diffusion stripes in transistor-level design.

Pseudo-NMOS Transistor-Level Single-Diffusion Design of Address Decoders



Transistor-Level Selectors / Multiplexers



CMOS Logic Structures

1. Conventional Logics
2. RAM/ROM-based Logic (dense, easily configurable)
3. Fully/Partially Complementary Logic (CMOS) (dense, LP)
4. BiCMOS Logic (improving drive, fanout)
5. NMOS-like Logic (high fanin, half transistor count)
6. Source Follower Pull-up Logic (SFPL, '92, improving speed)
7. Pass-Transistor Logic (PTL) (→1/4 count, Vt-drop)
8. Transmission-Gate Logic (TGL) (complemetary)
9. Clocked CMOS Logic (reducing glitch, speedup)
10. Dynamic CMOS Logic (speedup)
11. Domino Logic ('82)
12. Differential Cascode Voltage Switch Logic (DCVSL, '84, IBM)
13. True Single-Phase Clocked Logic (TSPC, '89)
14. Complementary Pass-Transistor Logic (CPL, '90)
15. Differential Domino CMOS Logic
16. MOS Current-Mode Logic (MCML, '96)

1. Conventional Logics

Bipolar Junction Transistor (BJT)

- Relay Logic
  - Ladder Diagram, incomplete logic
- Sequentially Accumulated (Computed) Logic
  - Input, calculated, and output in MCU; Very slow applications
- DRL (Diode-Resistor Logic)
  - Pulled by R, almost passive
- TDL (Transistor-Diode Logic)
- TRL (Transistor-Resistor Logic)
- TTL (Transistor-Transistor Logic)
  - Standardized, 0~0.4/2.8~5V
- ECL (Emitter-Coupled Logic)
  - Fast, high power dissipation
- Integrated Injection Logic
  - Basically, a Wired AND logic at the collector; 1972

2. RAM/ROM-based Logic

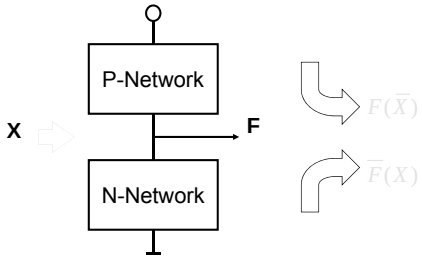
A Logic Unit in Some CPLD

ABC	W	X	Y	Z
000	0	0	0	0
001	0	0	1	1
010	1	0	0	1
011	1	0	0	0
100	0	1	0	0
101	1	0	0	0
110	0	0	1	0
111	0	0	0	1

- Universal but exponential size wrt. input count.
- Easily synthesizable
- Flexible and reconfigurable for both RAM and logics.
- Usually utilized in most CPLD.

3. Standard CMOS Logic Structures

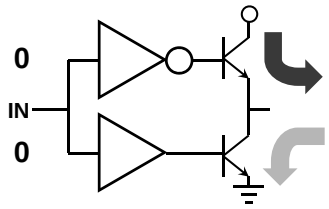
Complementary MOS Logic



4. BiCMOS Logic Structures

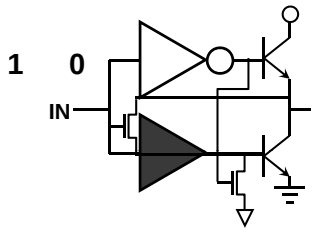
BiCMOS Logic

- Compared with Bipolar Logics:
  - CMOS Logics: Low power (IDDQ→0)
  - Poor drive capability
- Basic idea of BiCMOS Inverter:



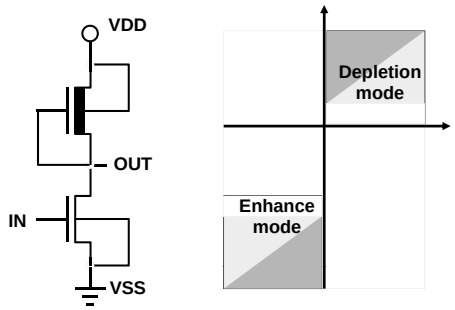
4. BiCMOS Logic Structures

A BiCMOS Inverter

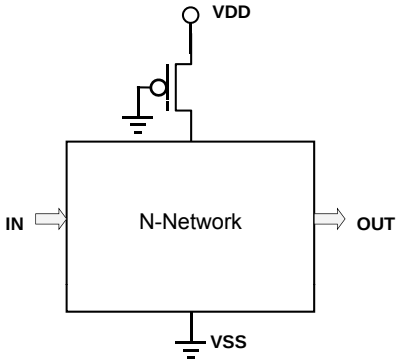


5. NMOS Logic Structures

NMOS Inverter

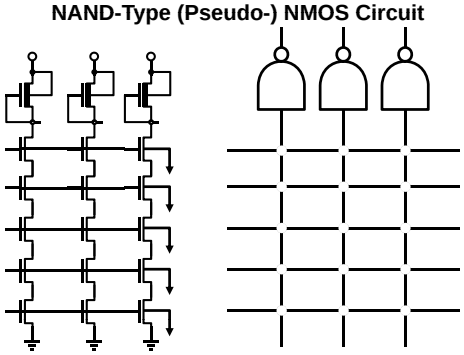


5. Pseudo-nMOS Structures



5. NMOS-like Structures

NAND-Type (Pseudo-) NMOS Circuit

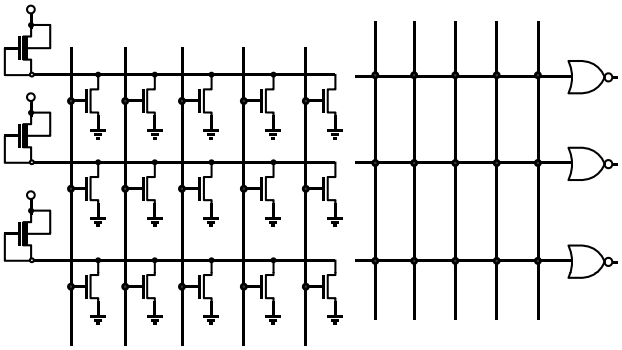


Body Effect!

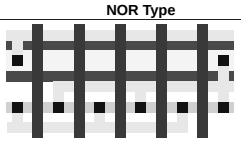
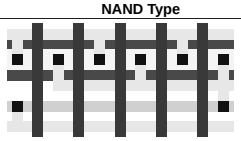
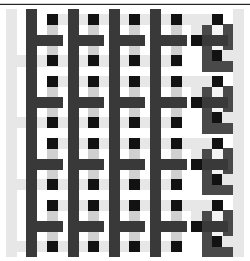
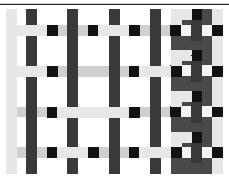
Compact, low-power but slower.

5. NMOS-like Logic Structures

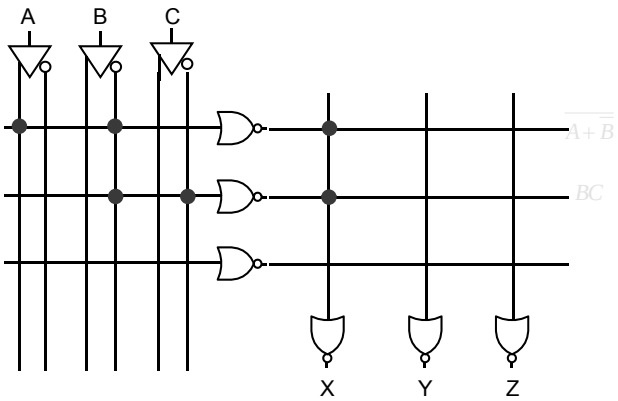
NOR-Type (Pseudo-) NMOS Circuit



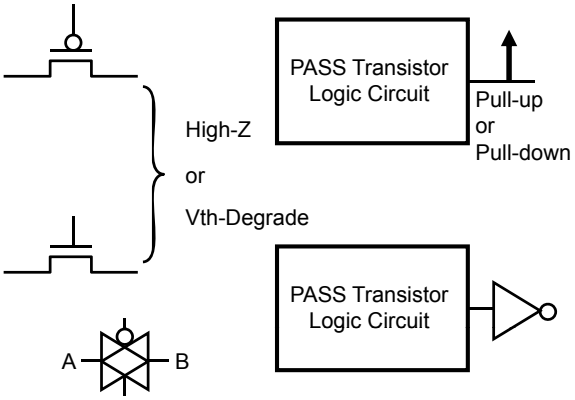
5. Compaction, Leakages & Speed

	NOR Type	NAND Type
CMOS		
NMOS-like		 + Low-area + Low-power + Low-cost - Low-speed

Programmable Logic Array (PLA)

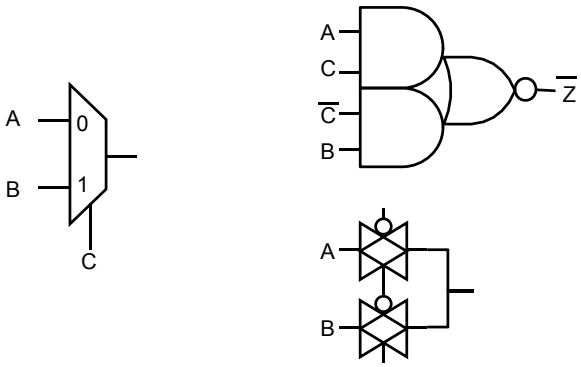


7. Pass-Transistor & Transmission Gate

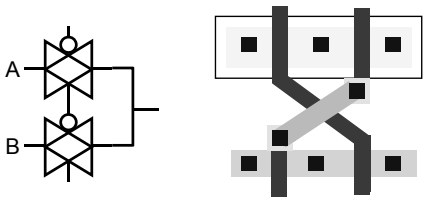


Multiplex

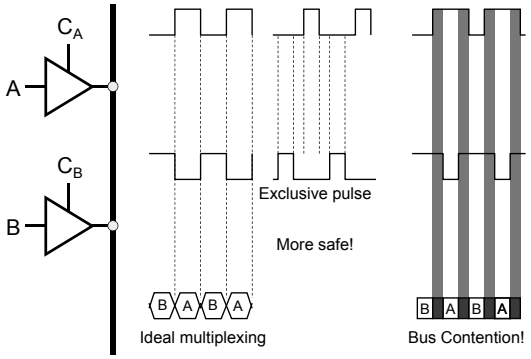
(review)



Multiplexer Layout



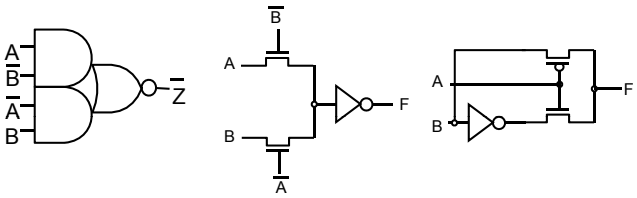
Bus Contention



Another problem in testing: difficult to test the control line stuck-at-1 faults.

PTL Exclusive OR Gate

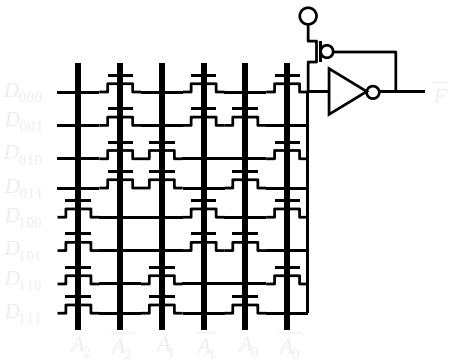
Pass-Transistor Logic Synthesis



1. **Popularly used in modulo-2 logic, such as ⊕ in LFSRs**
2. **Tradeoff btw speed, area and power-dissipation.**

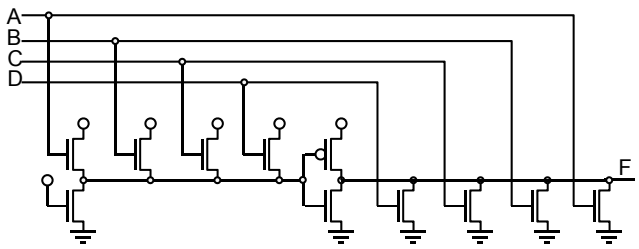
CMOS Logic Structures

Address Decoder using Pass Transistor Logic



6. SFPL

Source Follower Pull-up Logic

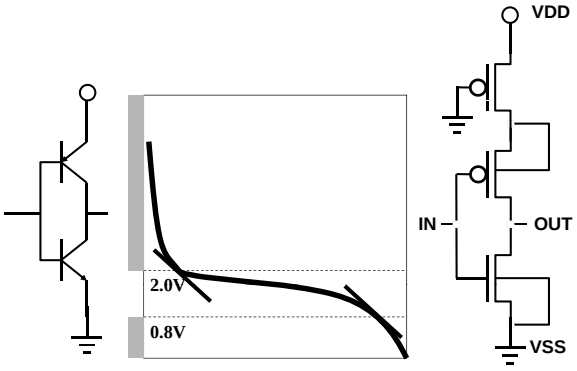


Fanin↗→Co↗

Discharging via Positive-Feedback at Inputs

CMOS Logic Structures

TTL-Interface Inverter



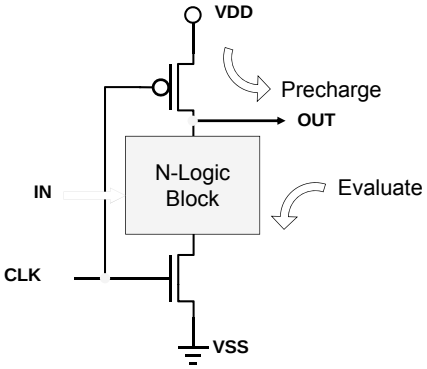
CMOS Logic Structures

General Dynamic CMOS Logic

- General Dynamic CMOS Logic:
  - IDD Path is turned off when clock-disabled and/or the output is evaluated when clock-enabled.
- In general:
  - Basic Dynamic CMOS n-Logic.
  - Basic Dynamic CMOS p-Logic.
  - Clocked CMOS Logic.
  - Domino Logic

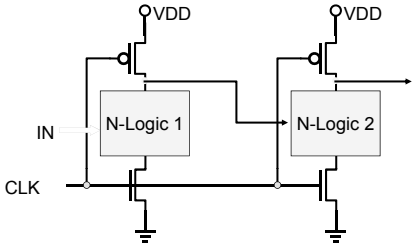
CMOS Logic Structures

Basic Dynamic CMOS Logic with n-Logic



CMOS Logic Structures

Erroneous Evaluation in Cascaded Dynamic n-Logics

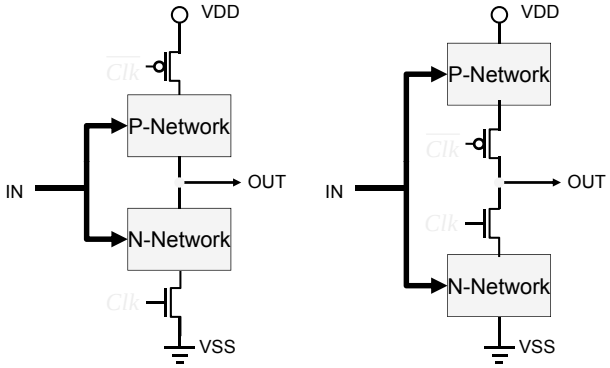


- They are evaluated at the same clock edges.
- Even slow evaluation may be impossible if the output has been discharged by pre-charged inputs.

➡ Complementary Clocked, Non-inverting or Zipper

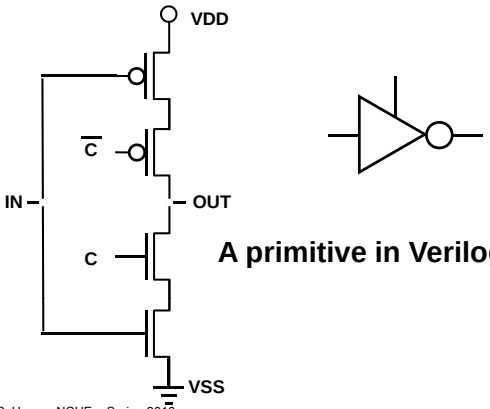
CMOS Logic Structures

Clocked CMOS Logic (C²MOS)



CMOS Logic Structures

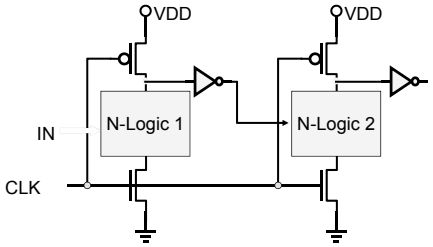
Tri-State Inverter



A primitive in Verilog: notif1

CMOS Logic Structures

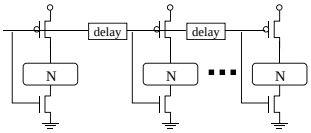
Domino Logic



- The output won't be discharged by pre-charged inputs.
- Evaluation (clock) time should be > t_r X #stages
- Limitations:
  - Buffer, non-inverting, charge redistribution

CMOS Logic Structures

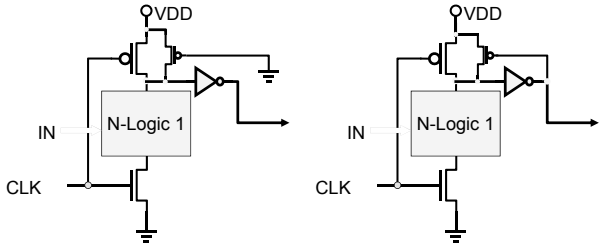
Wave Logic



- The timing is much critical.
- Very low immunity.

CMOS Logic Structures

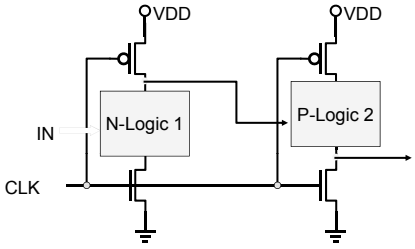
Domino Logic



- A weak pull-up p-device is used to balance the threshold and to make it static.
- The weak device is fed back -- a latch-version .

CMOS Logic Structures

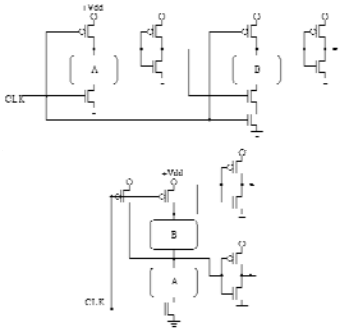
NP Domino Logic (Zipper CMOS)



- Dynamic circuit, small area, small parasitic capacitance;
- Glitch-free if designed carefully.

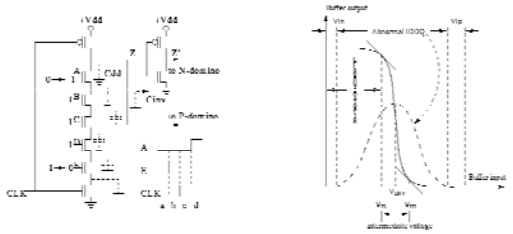
CMOS Logic Structures

Multi-output Domino Logic (MODL)



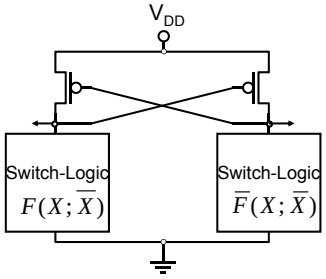
CMOS Logic Structures

Charging Sharing Problem in Domino Logic



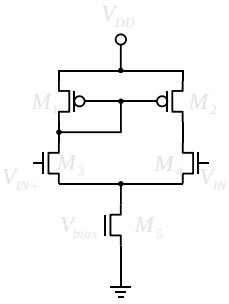
CMOS Logic Structures

Cascade Voltage Switch Ligic (CVSL)



- Can be minimized;
- Can be implemented in clocked version, wt pulled/latched devices.
- Good DC noise immunity => double railed for low voltage.

MOS Current-Mode Logic (CML)



Simple OTA

- The highest MOS logic recently (1996)
- CVSL and CML provide complement logc outputs.
- Differential pair operates either in the saturation or cut-off regions.
- Current switch occurs at the point of maximum transconductance for both MOSFETs.
- Propagation delay is proportional to the output swing, independent from the supply voltage.
- Constant amount of current is drawn from power supply, independent from the switching activity.
- Much more efforts on dedicate design comparable to the multiple stage OPA design!

MOS Current-Mode Logic (CML)

Example

A \ B	0	1
0	$\overline{F}$	$\overline{F}$
1	$\overline{F}$	F