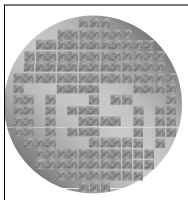


VLSI Design

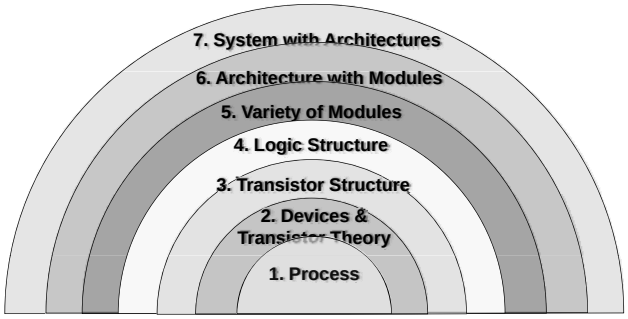
Tsung-Chu Huang

Department of Electronic Engineering
National Changhua University of Education
Email: tch@cc.ncue.edu.tw

2016/03/01

Syllabus Structure

Bottom-up Hierarchy



Transistor Power/Timing Models

Summary

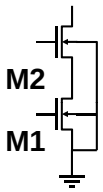
- Switch Models
  - ✓ Ideal Switch: Functional simulation without timing
  - ✓ Resistive Switch: Static power evaluation
  - ✓ Capacitive Switch: Dynamic power evaluation
  - ✓ RC Switch: Basic power and timing evaluation
- Transistor Structure Model
  - ✓ El More Model: loop RC additive.
  - ✓ Rabaey Model: Logical and branch efforts
- IDS Models
  - ✓ Shockley First-Order Equation: accurate manual derivation
  - ✓ Sub-threshold Models
- SPICE Models
  - ✓ Complicate Simulation

Transistor Network

Relay Logics

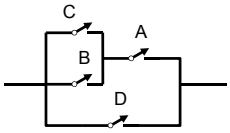
- **Stack Effect**
  - ✓ Parallel Switch: $S_{on} = A_{on} + B_{on}$, $R_s = R_A // R_B$
  - ✓ Serial Switch: $S_{on} = A_{on} \cdot B_{on}$, $R_s = R_A + R_B$
  - ✓ Parallel Capacitors: $C = C_A + C_B$
- **Body Effect**
  - ✓ is the threshold voltage changing of source-bulk voltage due to transistor connection in series.

$$V_{t2} \approx V_{t2} + 0.6\sqrt{V_{DI}}$$

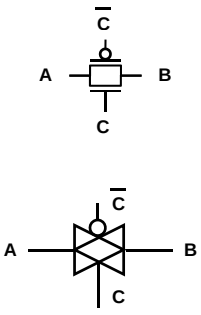


Logic Completeness and Switch

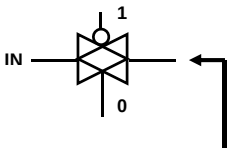
1. **{And, Or, Not} is a complete logic set.**
2. **A logic set is complete if and only if it can combine to all functions of another complete logic set, such as {NAND} and {NOR}**
3. **A basic relay (switch) logic can represent either AND or OR function only.**
4. **Example: F=A(B+C)+D**



Transmission Gate



Tri-State



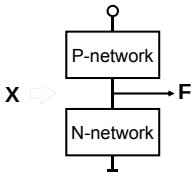
High Impediance
Floating (connection)
Hi-Z
'z'

Tri-State Logic

AND	0	Z	1
0	0	0	0
Z	0	Z	Z
1	0	Z	1

OR	0	Z	1
0	0	Z	1
Z	Z	Z	1
1	1	1	1

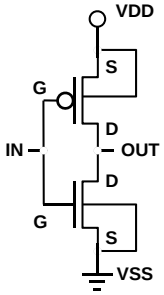
CMOS Logic

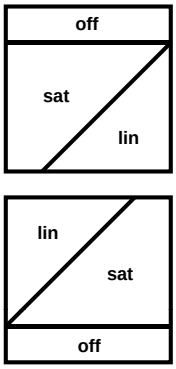


1. **N network is a relay logic of $\overline{F(X)}$**
2. **P network is a relay logic of $F(\overline{X})$**

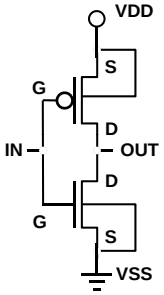
} AND←→OR

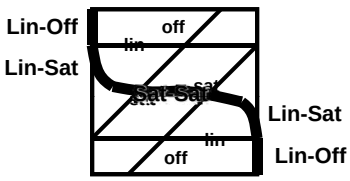
Transfer Function of CMOS Inverters





Transfer Function of CMOS Inverters





Lin-Sat Curve is a little complicate (skipped), but Sat-Sat seems simple!

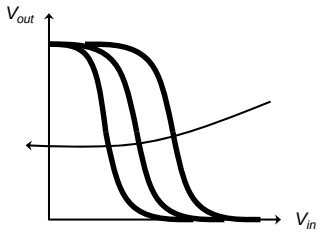
Transfer Function of CMOS Inverters

Inverter Size = S = $\frac{\beta_n}{\beta_p} = \frac{\mu_n}{\mu_p}\frac{W_n}{L_n}\frac{L_p}{W_p} \approx 2.6\frac{W_n}{L_n}\frac{L_p}{W_p}$

Inversion Voltage: = $V_{inv} = \frac{V_{DD} + V_{tp} + V_{tn}\sqrt{S}}{1+\sqrt{S}}$

Unit-size & Equal-inversion: $V_{inv} = \frac{V_{DD}}{2}$

Beta-Ratio Effects

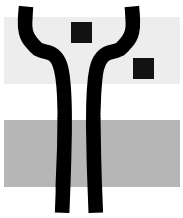


Unary-Sized Inverter

Inverter Size = S = $\frac{\beta_n}{\beta_p} \approx 2.6 \frac{W_n}{L_n} \frac{L_p}{W_p}$

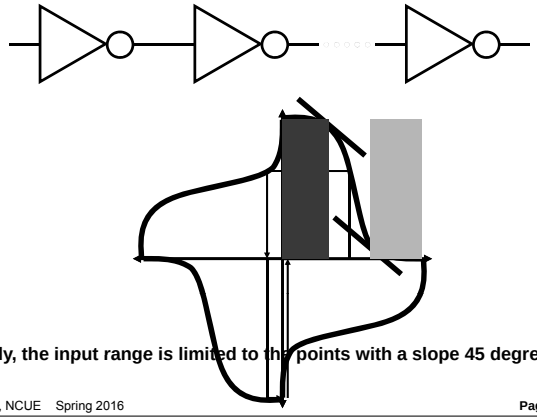
When $Lp=Ln=L$, $W_p : W_n \approx 2.6:1 \approx 2$

PS. Usual Layout Skill:



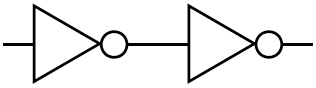
Min.-Size: $L=Lmin,\ W=Wmin$

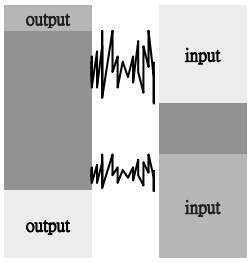
Identical Inverter Cascade



Usually, the input range is limited to the points with a slope 45 degrees.

Noise Margin



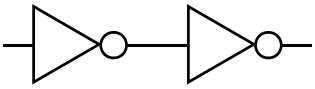


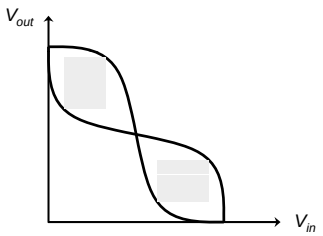
$NM_H = V_{OHmin} - V_{IHmin}$

$NM_L = V_{ILmax} - V_{OLmax}$

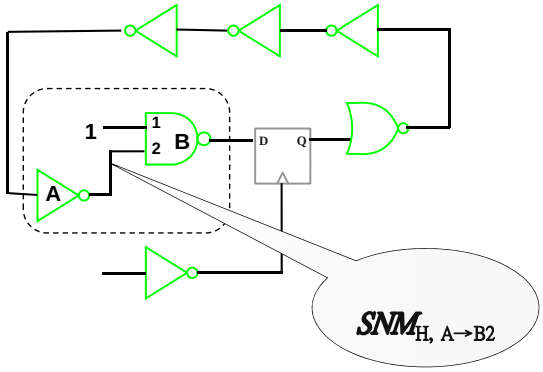
Butterfly Chart

Representing Static Noise Margins

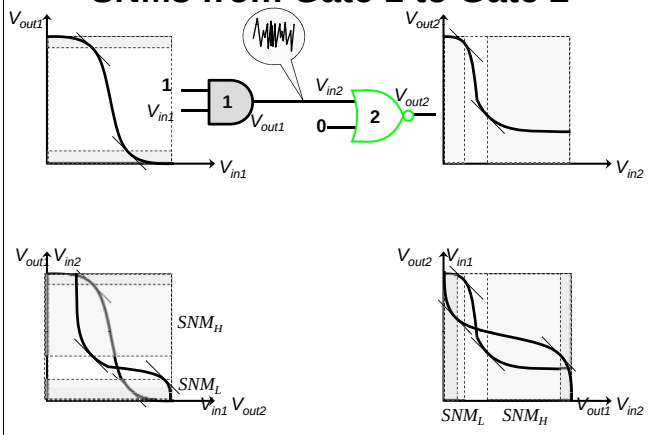




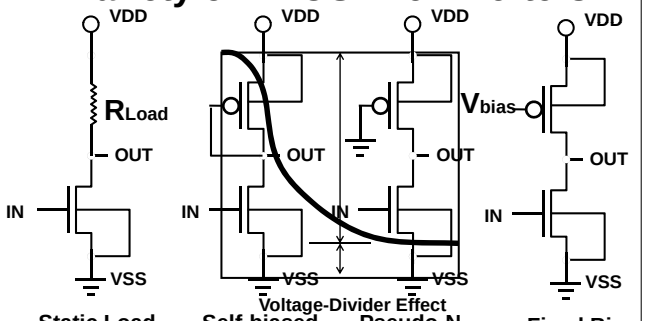
SNMs Everywhere !



SNMs from Gate 1 to Gate 2



A Variety of nMOS-like Inverters

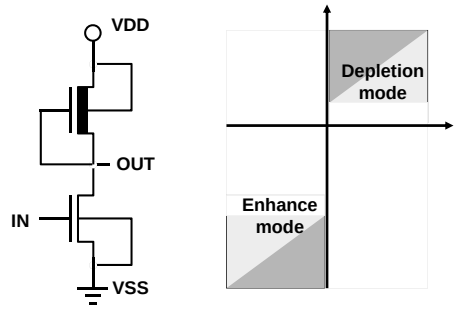


Typically Sizing: $R_{on} << R_{Load} << R_{off}$

Equal-Ratio Sizing: $R_{on} : R_{Load} = R_{load} : R_{off}$

Speed-Compromised Sizing: $R_{Load} = kR_{on}$, k~4 for large R_{off}

NMOS Inverters

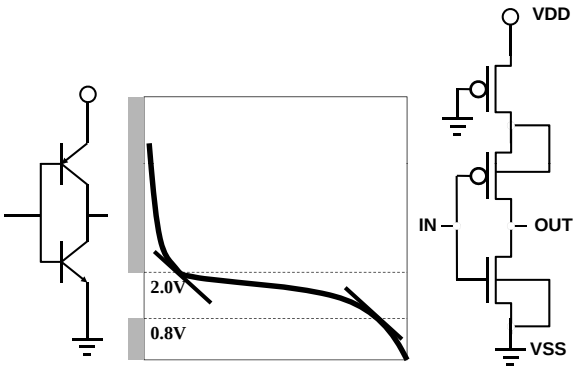


Transistor Sizing for Equal-Inversion

- Assume $V_{tn} = |V_{tp}| = V_{DD}/5$, and $V_{tn} = -3V_{DD}/5$ in NMOS enhancement mode:

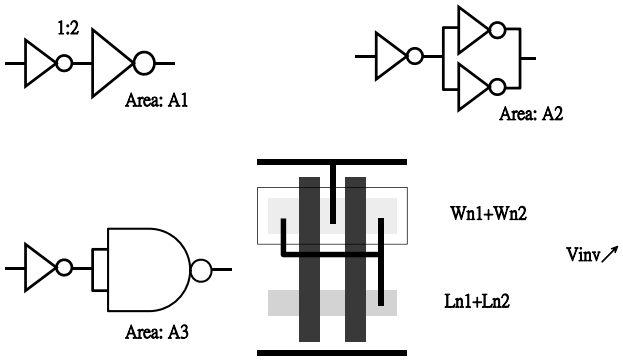
Inverter	Inverter Size
CMOS	1:2.5
NMOS	4:1
Pseudo-N	2.5:1

TTL-Interface Inverter

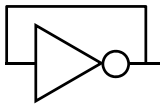


Stacking along Diffusion Lines

Example: considering a buffer with a stage ratio of 2

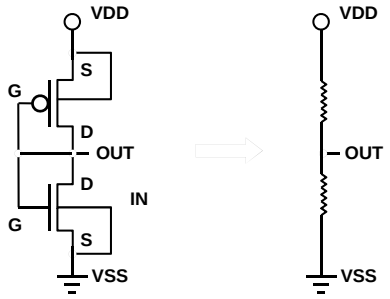


Myth: 180˚Oscillator?



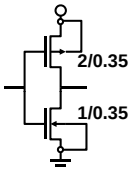
...010101010101

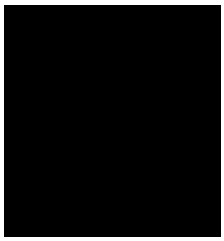
In fact,



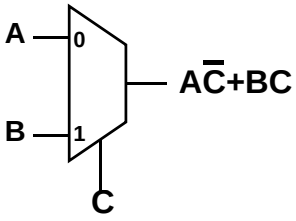
Stick Diagram

1. **Representations of Layout**
   - **Grid-base graph**
   - **EDIF: hierarchical language with coordinates.**
   - **Stick diagram: for sketch or plan**
2. **Example：**

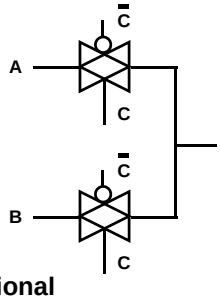




2-to-1 Multiplexer



TG-based Multiplexer



Bidirectional

No tri-state in ideal timing

Bus Contention possibly !

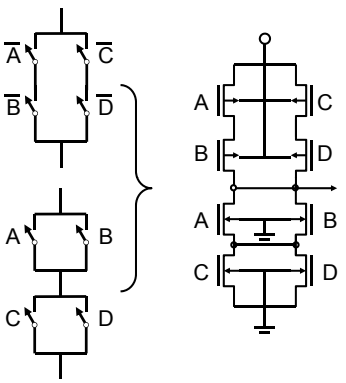
Example：$F=\overline{(A+B)(C+D)}$

$F=\overline{A}\,\overline{B}+\overline{C}\,\overline{D}$

P network：

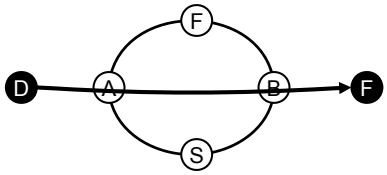
$\overline{F}=(A+B)(C+D)$

N network：

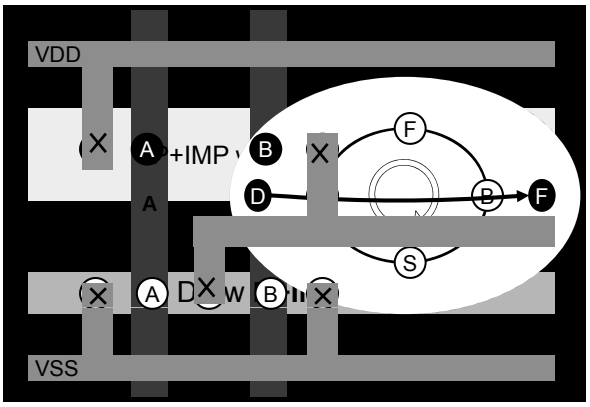


Euler Path

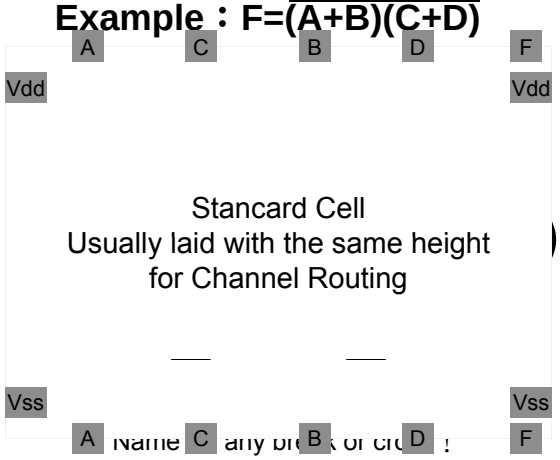
1. Topology in 18th Century Applied in CMOS
2. N path: Relay logic of N network
3. P path: Relay logic of P network
4. N path crosses p path at input X and $\overline{X}$.



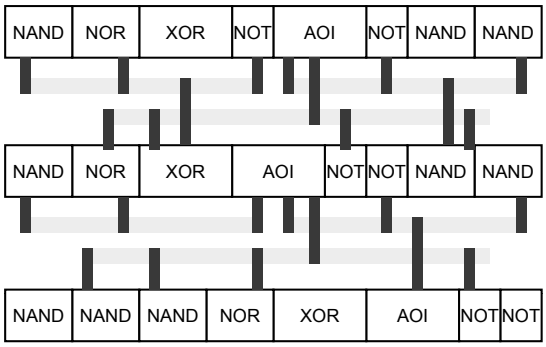
Euler Path Guided Layout



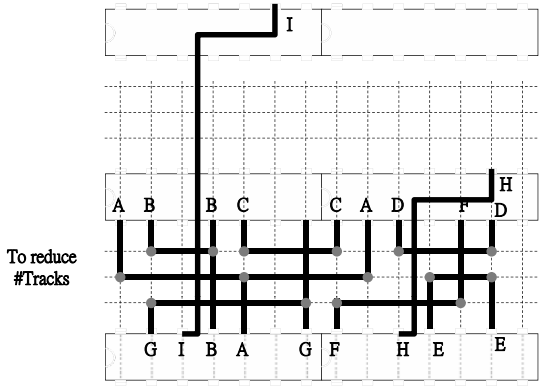
Example : F=$\overline{(A+B)(C+D)}$



Cell-Based Channel Routing

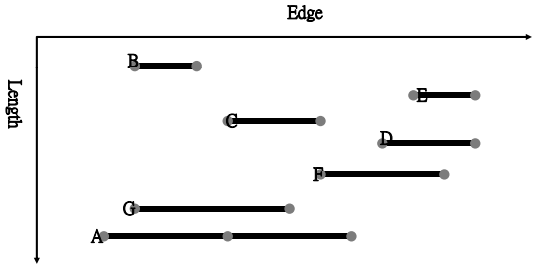


Channel Routing



LEA: Left-Edge Algorithm

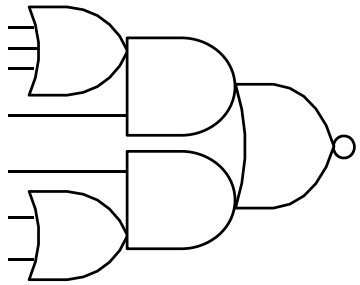
1. Sort by length
2. Select from Left Edge



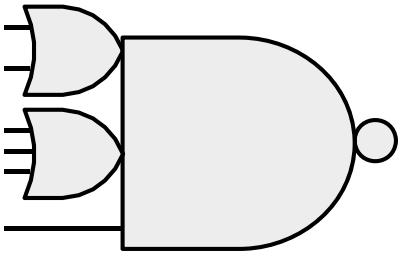
Primitive Gates

1. Primitive: A-tomic (Cannot be cut off)
2. Properties of a CMOS Primitives:
   - Either pulled up or pulled down;
   - Current from or to the single output
   - IDDQ=0 for Ideal CMOS
3. Usual Symbols:
   - directly assembled without wire.
   - {AND, OR} Combo ended with an Inverter

Complex Primitive Trivial Example

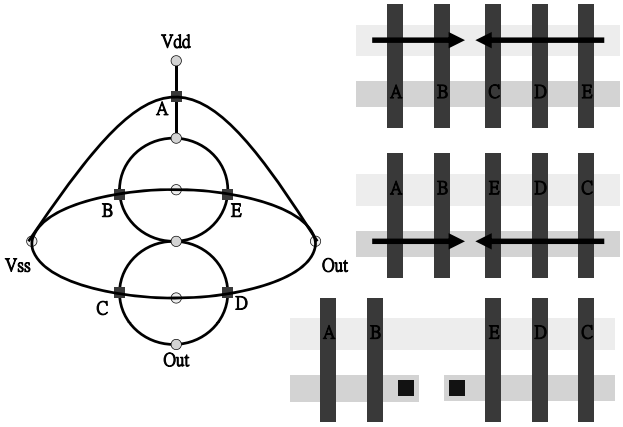


Usual Example and Naming



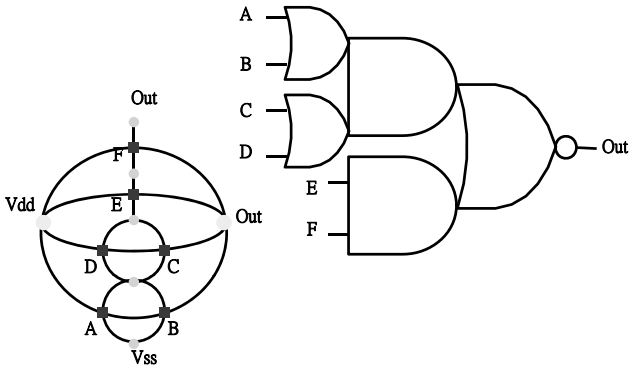
OAI231

Interlaces of Diffusion Lines



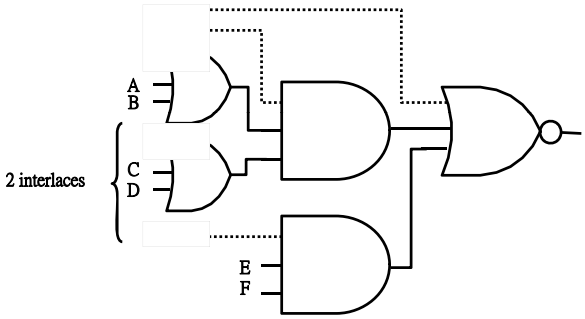
Minimum Interlace Algorithm

Example: $\overline{Out=(A+B)(C+D)+EF}$



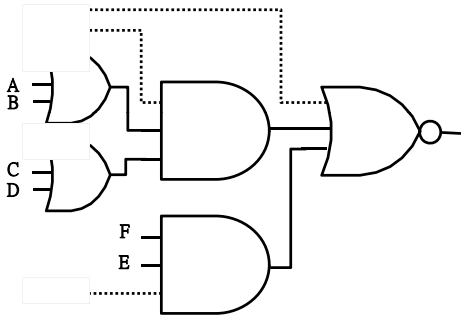
Minimum Interlace Algorithm

- Adding a pseudo input to each sub-gate such that each sub-gate has odd inputs.

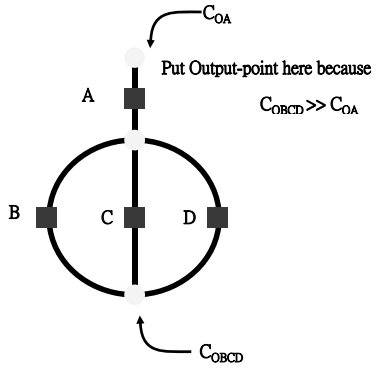


Minimum Interlace Algorithm

- Rotate each axis to reduce the inner interlaces

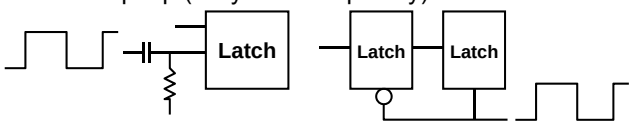


Output Capacitance Minimization

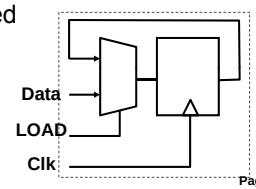


Memory – Latches and Registers

- Prior to '90s, they're used to be confused.
- ➢ Latch: Level Sensitive
- ➢ 50's Flipflop (Very slow frequency):



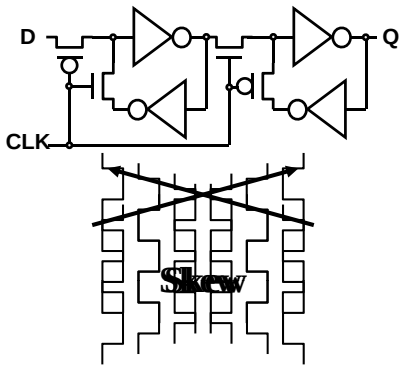
- ➢ Later Flipflop: Edge Triggled
- ➢ Register: Loadable or Hold



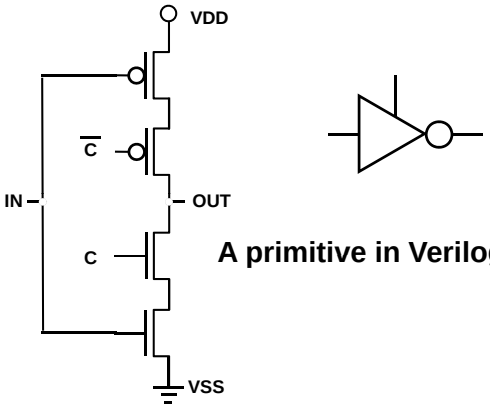
Static Gate Based Latch

Example: Resettable D Latch

Switch-Based Static Latch and Flipflop



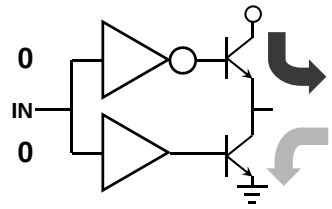
Tri-state Inverter



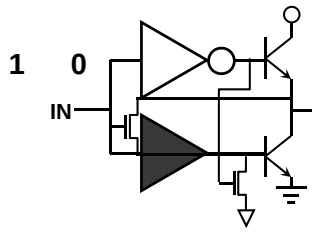
A primitive in Verilog: notif1

Basic Concept on BiCMOS Inverters

- Compared with Bipolar Logics:
  - CMOS Logics: Low power (IDDQ→0)
  - Poor drive capability
- Basic idea of BiCMOS Inverter:



BiCMOS Inverter



Transistor Sizing & Reordering

- Minimizing Area
- Maximizing/Equalizing Noise Margin
- Minimizing/Equalizing Rising & Falling Time
- Minimizing Propagation Time
- Minimizing Power Dissipation
- Reducing Glich
- Minimizing Charge Sharing Effect
- Increasing Regularity for EDA

Roughly Area Estimation

- In several synthesis tools (2000):
  An N-input CMOS Primitive Cell:
  (0.5+0.5N) units (compared to a unit inverter)
- Dependent on Layout Style

NMOS Logic Array