國立彰化師範大學電子系 108 學年第 2 學期

「超大型積體電路設計導論」期末專題報告

全訂製佈局設計流程

題目：設計一 CMOS 反相器，依完整標準流程項目鍵入並貼上親自上機相關畫面，儲存前以工具壓縮圖片方便電子郵寄。於 2020/6/30 前 Email 至老師信箱，兩日內沒收到回條請與老師聯繫。

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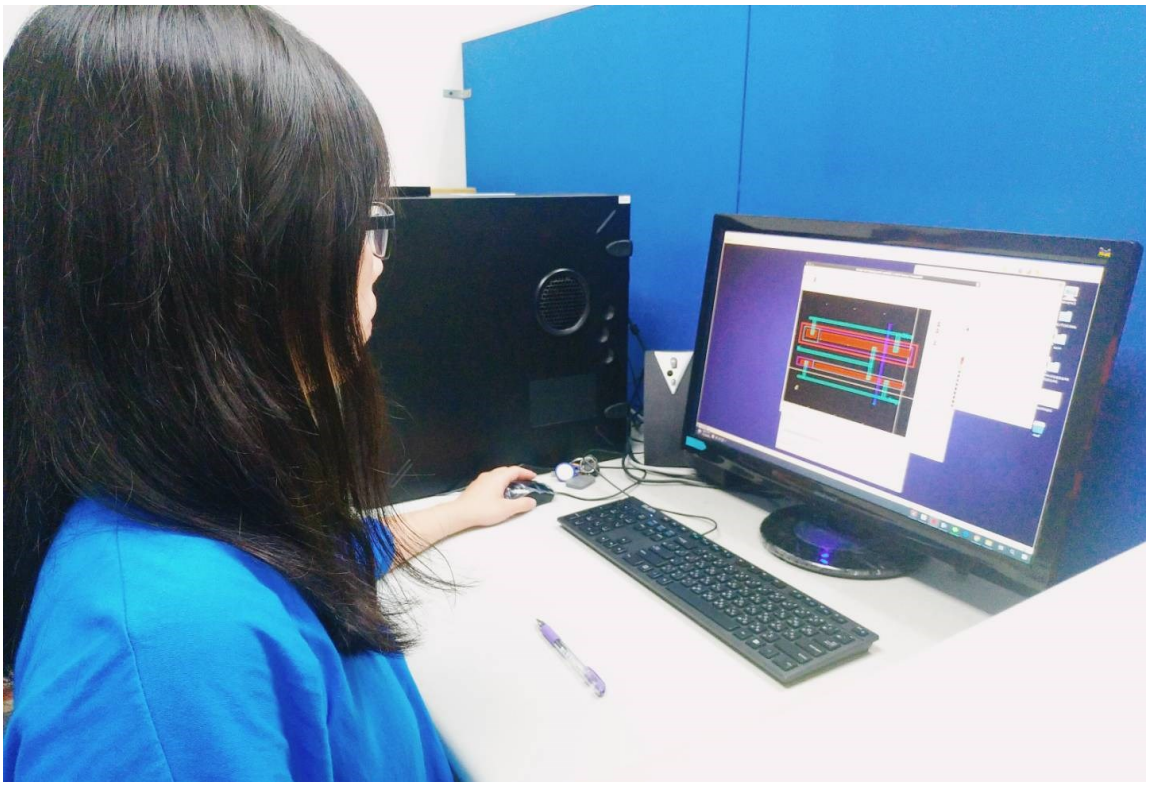
日期：20200611



I. 自行完成專題保證：以 50 字以內說明獨自完成之聲明。

本專題個人認為是最早開始製作的，每次花一小段時間做，長期完成，過程中也幫助過許多同學，因此可保證此專題是本人親力親為的專題。

II. NM 或 Putty/Xming 安裝設定步驟

1.從老師雲端下載 NX 壓縮檔

2.解壓縮並執行所有 exe 檔

3.打開 NX Connection 設定

4.在 session 設定名稱(自行定義)、Host 打入 IP 位址 120.107.171.186、Port 為 5903、internet connect 設定為 ADSL, 按 Next

5.設定 Unix, GNOME, 按 Next

6.將 Show the Advanced Configuration dialog, 按 Finish

7.按 key, 按 Import 匯入 NX.key, 按 save

8.按 Advance 標籤，將”Disable DirectDraw for screen rendering”打勾，按 save，完成設定

III. 常見 Linux 指令說明(最少 10 個)

1.pwd:顯示所在的目錄

```
[s0653037@ncue851 cic18]$ pwd
/home/s0653037/work/cic18
```

2.ls:顯示檔案內容

```
[s0653037@ncue851 cic18]$ ls
CIC18LIB  NewLab              calibre         inv_CDL_netlist.sp   run_cdb2oa.csh
Hw        PAD                 cdb2oa.gui.log  inv_CDL_netlist.sp~  sample
Lab       PIPO.LOG.inv        cds.lib         libManager.log       si.env
Lab_PEX   PIPO.SUM.inv        cic18.tf        map                  si.foregnd.log
Lab_drc   aoi_CDL_netlist.sp  display.drf     model                si.log
Lab_lvs   aoi_CLD_netlist.sp  ihnl            netlist              term_project
MyLab     aoi_CLD_netlist.sp~ inv.calibre.db  raw                  tmpCphMsg
```

3.which:搜尋執行檔

```
[s0653037@ncue851 term_project]$ which hspice
/usr/cad/synopsys/hspice/cur/hspice/bin/hspice
```

4.clear:清除螢幕畫面

```
[s0653037@ncue851 term_project]$ clear
```

5.passwd:更改密碼

```
[s0653037@ncue851 cic18]$ passwd
Changing password for user s0653037.
Changing password for s0653037.
(current) UNIX password:
New password:
Retype new password:
passwd: all authentication tokens updated successfully.
```

6.cat:將檔案內容列出

```
[s0653037@ncue851 cic18]$ cat .cshrc
cat: .cshrc: No such file or directory
[s0653037@ncue851 cic18]$ cd
[s0653037@ncue851 ~]$ cat .cshrc
#!/bin/tcsh
echo "********Please source what you want********"
sh /usr/cad/echo.cshrc
echo "********Please source what you want********"
echo "********EXECUTED********"
echo "source /usr/cad/cadence/CIC/ic_06.15.151.cshrc"
source /usr/cad/cadence/CIC/ic_06.15.151.cshrc
echo "source /usr/cad/mentor/CIC/calibre.cshrc"
source /usr/cad/mentor/CIC/calibre.cshrc
echo "source /usr/cad/synopsys/CIC/hspice.cshrc"
source /usr/cad/synopsys/CIC/hspice.cshrc
echo "alias dv 'design_vision'"
alias dv "design_vision"
echo "alias dc 'dc_shell'"
alias dc "dc_shell"
echo "********EXECUTED********"
echo "Please edit .cshrc to make it better to use"
```

7.more:檔案內容太大，使用 cat 時無法將檔案內容全部列出，用 more 即可看到未列出的部分

```
[s0653037@ncue851 inv]$ more *.lis
::::::::::::::
inv.postSim.lst.lis
::::::::::::::
 ****** HSPICE -- P-2019.06 linux64 (May 26 2019) ******
  Copyright (c) 1986 - 2020 by Synopsys, Inc. All Rights Reserved.
  This software and the associated documentation are proprietary
  to Synopsys, Inc. This software may only be used in accordance
  with the terms and conditions of a written license agreement with
  Synopsys, Inc. All other use, reproduction, or distribution of
  this software is strictly prohibited.
  Input File: inv.postSim.sp
  Command line options: /usr/cad/synopsys/hspice/cur/hspice/linux64/hspice -i inv.postSim.sp -o inv.p
ostSim.lst
  Start time: Wed Jun 10 23:41:44 2020
 lic:
 lic: FLEXlm: SDK_12.2
 lic: USER:   s0653037             HOSTNAME: ncue851
 lic: HOSTID: 3497f6831da9         PID:      22773
 lic: Using FLEXlm license file:
 lic: 26585@lscic
 lic: Checkout 1 hspice
 lic: License/Maintenance for hspice will expire on 14-may-2022/2020.03
 lic: 182(in_use)/250(total) FLOATING license(s) on SERVER 26585@lscic
 lic:
  **warning** (/home/s0653037/work/cic18/model/cic018.l:454) Model n_18 device geometries will not be
 checked against the limits set by lmin, lmax, wmin and wmax. To enable this check, add a period(.) t
o the model name(i.e. enable model selector).
  **warning** (inv.pex.netlist.sp:7) Global net name "gnd" in subckt pin list. The pin will be connec
ted to the local net. Recommend to not use global net names in subckt pin lists.
1****** HSPICE -- P-2019.06 linux64 (May 26 2019) ******
 ******
--More--(4%)
```

8.cd:進入指定的路徑

```
[s0653037@ncue851 cic18]$ cd term_project/
[1]    Done                          virtuoso
[s0653037@ncue851 term_project]$ clear
```

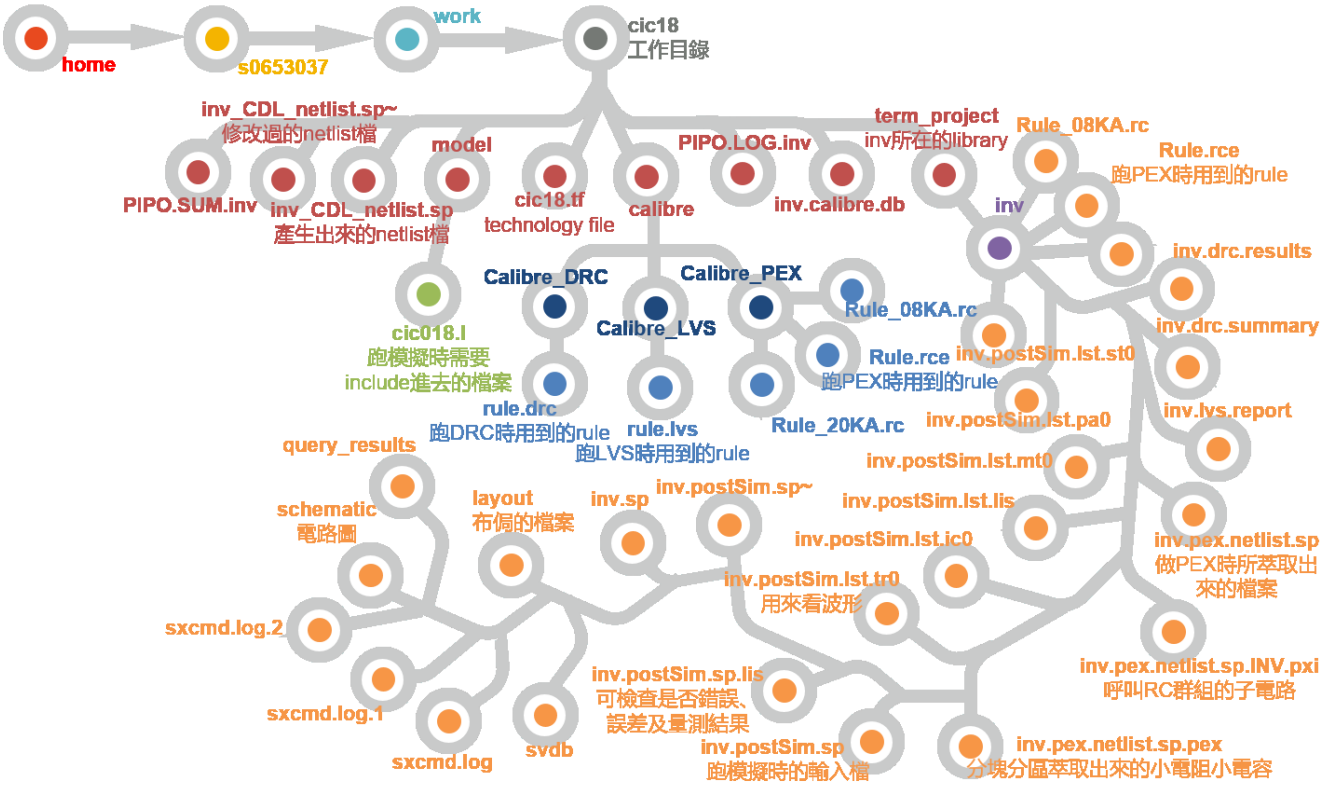
9.history:查之前所使用過的指令

```
[s0653037@ncue851 term_project]$ history
     1  15:20   source /usr/cad/synopsys/CIC/primetime.cshrc
     2  15:25   ~cd
     3  15:54   more MyLab.layermap
```

10.alias:可幫指令另取別名。

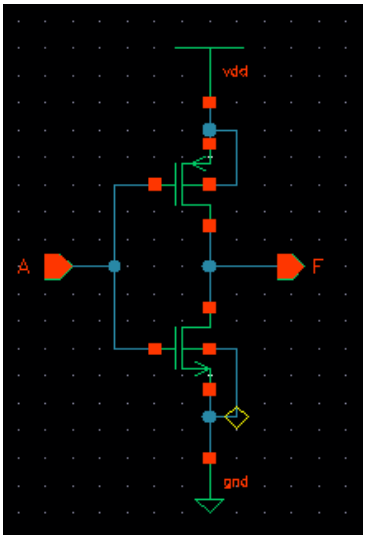
```
[s0653037@ncue851 term_project]$ alias clr='clear'
```

IV. 畫樹狀圖說明所需檔案結構並簡要說明檔案用途。



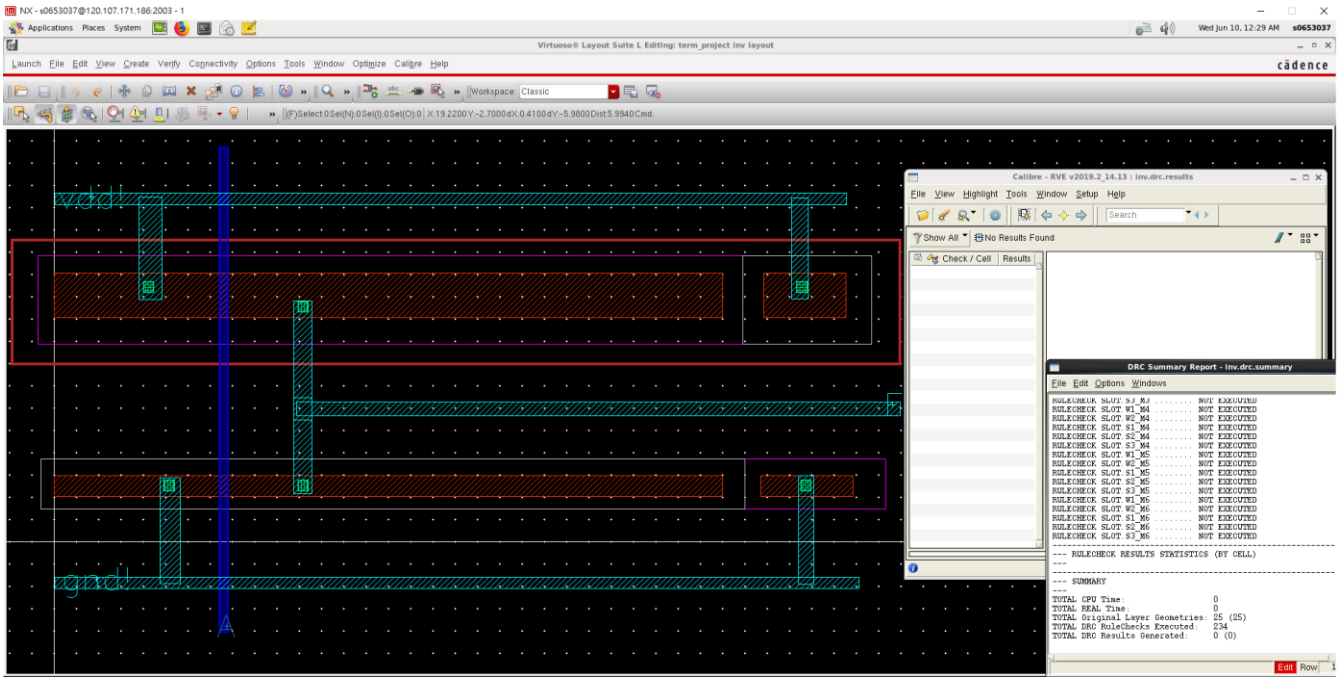
V. 假設 Lp=Ln=0.18um, Wp=1um, Wn=0.47um 設計 Inverter, 先畫 Schematic 流程，要做到 Check & Save, 及 Export to CDL 備用。(細部流程自行編號)

1. 進入 virtuoso
2. 建立一個新的 Library(名稱為 term_project)
3. 建一個新的 cell view,Schematic(名稱為 inv)
4. 擺放元件。按快捷鍵 I。vdd 和 gnd 的 Library 在 analogLib，PMOS 和 NMOS 在 CIC18LIB，選擇 P_18 及 N_18，MOS 需要調整寬度(Wp=1um, Wn=0.47um)
5. 按快捷鍵 W 接線
6. 按 P 放輸入(Pin Names:A)及輸出(Pin Names:F)
7. Check and Save
8. 到 CIW，Export to CDL，放在同一 Library(term_project)，名稱為 inv_CDL_netlist.sp
9. 輸入 ls 確認是否產生 inv_CDL_netlist.sp
10. 輸入 gedit inv_CDL_netlist.sp 修改檔案，將 GLOBAL 前面的星號拿掉之後儲存

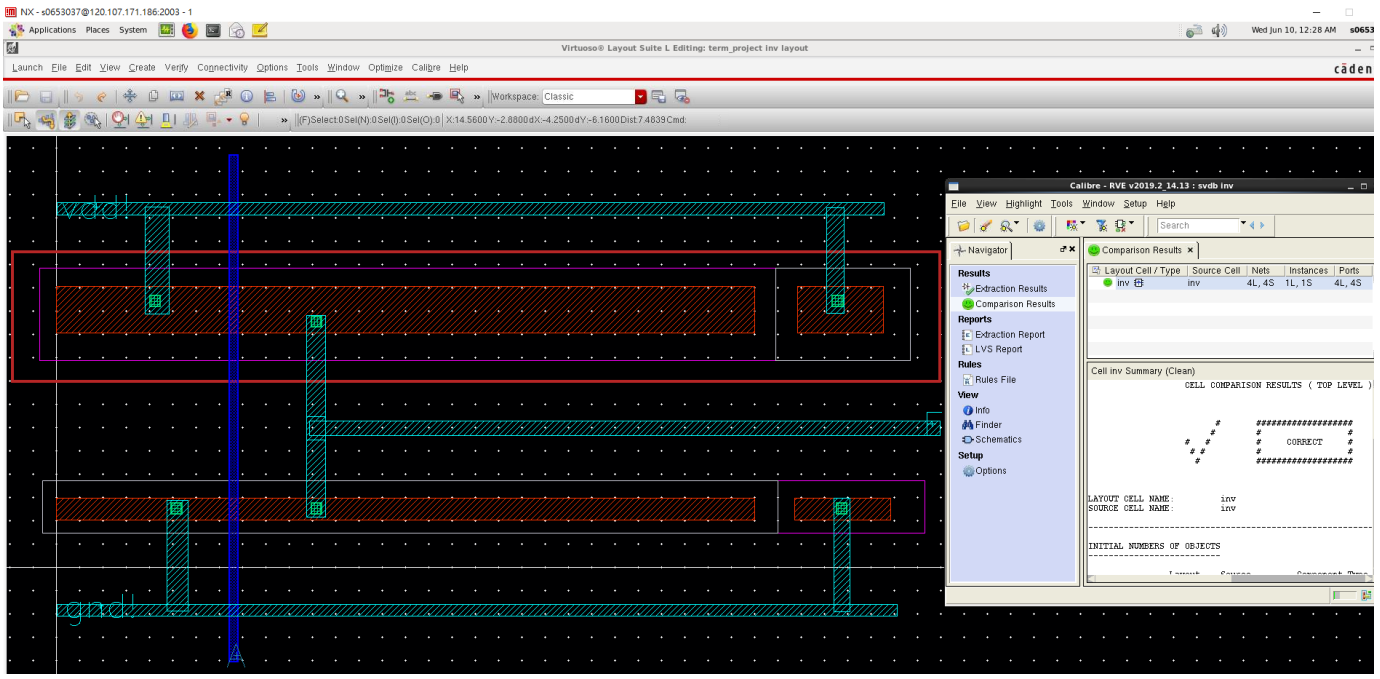


VI. 以 Cadence Virtuoso 佈局，完成 DRC/LVS 和 PEX。

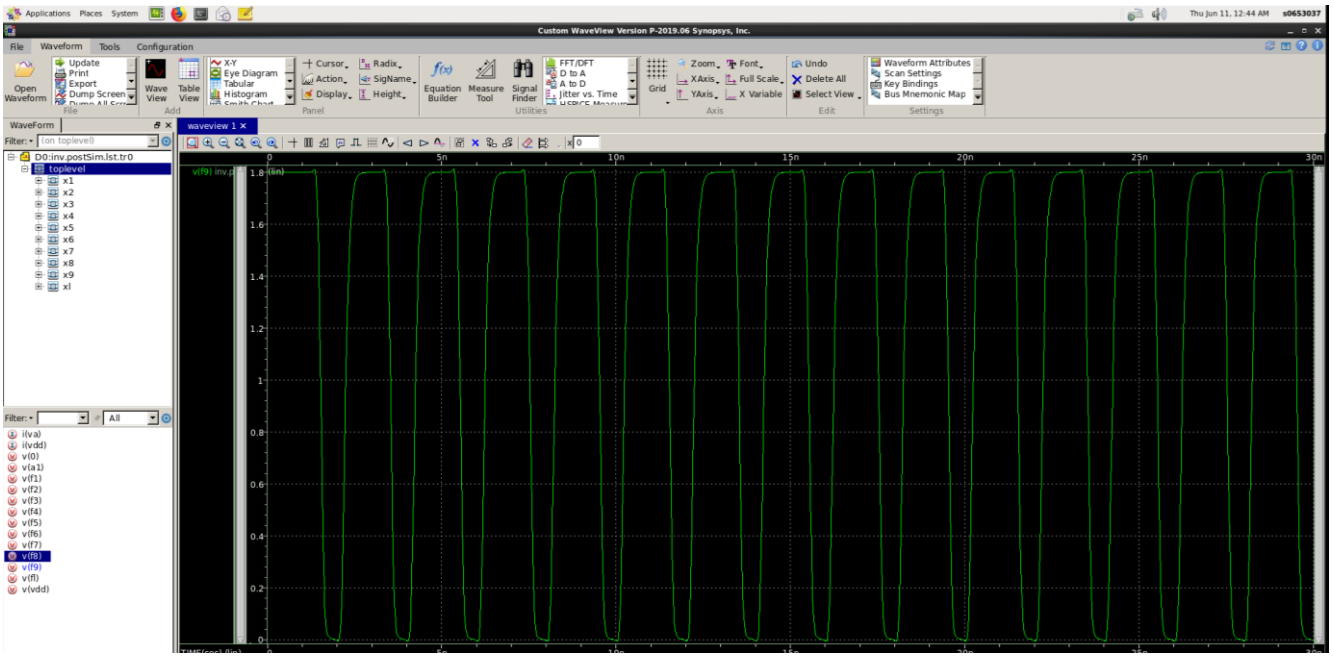
DRC



LVS



VII. Post-Layout HSPICE Simulation，以.MEAS 量測 10-Inverter Cascade 中第 9 個的第 10 個上升延遲時間，貼上 WaveView (wv) 脈波圖及圈出 List 檔中延遲時間。




```
s0653037@ncue851:inv
File  Edit  View  Search  Terminal  Help
...skipping

 ****** transient analysis tnom=  25.000 temp=  25.000 ******
tr9= 255.5013p  targ=  20.3911n   trig=  20.1356n

          ***** job concluded
 ******
 * postsim for inv gate

 ****** job statistics summary tnom=  25.000 temp=  25.000 ******

 ******  Machine Information  ******
 CPU:
 model name      : Intel(R) Core(TM) i7-6700 CPU @ 3.40GHz
 cpu MHz         : 800.000

 OS:
 Linux version 2.6.32-754.27.1.el6.x86_64 (mockbuild@x86-02.bsys.centos.org) (gcc version 4.4.7 20120
313 (Red Hat 4.4.7-23) (GCC) ) #1 SMP Tue Jan 28 14:11:45 UTC 2020


  ******  HSPICE Threads Information  ******

  Command Line Threads Count :      1
  Available CPU Count        :      8
  Actual Threads Count       :      1


  ******  Circuit Statistics  ******
  # nodes       =     413 # elements   =     552
  # resistors   =     360 # capacitors =     170 # inductors   =       0
  # mutual_inds =       0 # vccs       =       0 # vcvs        =       0
  # cccs        =       0 # ccvs       =       0 # volt_srcs   =       2
  # curr_srcs   =       0 # diodes     =       0 # bjts        =       0
  # jfets       =       0 # mosfets    =      20 # U elements  =       0
  # T elements  =       0 # W elements =       0 # B elements  =       0
--More--(97%)
```

VIII.學習心得 (100 字以內)

這次的專題讓我真正了解到佈局的所有過程，我覺得這些東西很複雜，感覺我們這次的專題只是這些知識的一些皮毛。雖然過程中非常累，但是能夠擁有這麼好的資源去學習，我們真的很幸福!而這些東西也確實值得我們去花很多的時間去研究!