**Homework #1**

Dept. Electronics Eng., Nat’l Changhua Univ. of Edu. Due Date: 2022/4/11

(You can upload the pdf by print/handwrite/scan, paste any handwritten picture, or directly answer in MS Words.)

Reg. No.：\_\_\_\_\_\_\_\_\_\_\_\_\_\_ Student’s Name：\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

1. TRUE OR FALSE (Mark ○ or X, 20%):

( ) 1. The linearity of the IDS model in the linear region reflects in the gm function of VDS.

( ) 2. Linux’s command *which* is similar to DOS command *where*.

( ) 3. The smallest oscillator can be implemented by connecting the output of a CMOS inverter to its input.

( ) 4. The .mt# files out of SPICE simulation can be read by EXCEL without Matlab-Hspice toolbox.

( ) 5. SKILL is a CAD scripting language for most Cadence’s tools.

( ) 6. Preventing from the latch-up effect the n-well should be biased to ground.

( ) 7. For a SPICE netlist the transfer function can be simulated by .AC.

( ) 8. FinFet and 3D-IC are two major infrastructures for retaining the Moore’s Law.

( ) 9. A typical layout includes four steps including floor-planning, partitioning, placement and routing.

( ) 10. The cascade-inverter driver line can be optimized with a stage ratio about 63%.

1. MULTIPLE CHOICE (Choose the best one, 20%):

( ) 1. Which effect may cause noise margin loss for stacked transistors in a gate? (A) stack (B) antenna (C) latch-up (D) body.

( ) 2. Which diagram can be better to present the dynamic noise margins? (A) Butterfly (B) Eyes (C) Bode (D) Lissajous.

( ) 3. The transfer function of the circuit XOR(NAND(A,A), NOR(A,A)) looks like (A)┌┘ (B) -\_- (C) \_─\_ (D)└┐.

( ) 4. Which power dissipation is most sensitive to the supply voltage? (A) static current (B) dynamic power (C) short current (D) subthreshold current.

( ) 5. Minimizing delay of a L=1mm wire with delay = (L/1um)2 ps, how many 2ns-buffers are inserted? (A)11 (B)21 (C)31 (D)41.

( ) 6. Which shape of active region is better for matching layout? (A) bd (B) bp (C) bb (D) bq.

( ) 7. Initials of Poly, Metal, Diffusion, Oxide mean their sheet resistances; (A) P>M>D>O (B) O>D>P>M (C) O>D>M>P (D) M>P>D>O.

( ) 8. In SPICE the Bode plot is often obtained by simulation (A) .AC (B) .DC (C) .TRAN (D) .TF

( ) 9. Which is not a purpose of growing poly-silicon prior to iron implementation, (A) serving as a mask (B) preventing from latchup (C) working as a transistor gate (D) self-alignment.

( ) 10. The tape-in procedure usually means submitting your layout to the (A) foundry (B) NSC (C) MOE (D) TSRI.

1. QUESTIONS (60%):
	* 1. Draw the stick diagram of the AOI22 CMOS gate F = $\overbar{ABC+D}$ in a Euler-path single-diffusion-line layout style. (10%)
		2. For a CMOS inverter with where k is p or n indicating the carrier type. Derive the input inversion voltage *Vinv* at *VDD*/2. (10%)
		3. Give a CMOS inverter and write a SPICE program with a piecewise-line voltage source to find its step response. (10%)
		4. Size the following gates according to Logical-Effort Model. The delay of a unitary inverter with an identical load is assumed to be 1. Let the intrinsic delay of an n-input gate be (n+1)/2. Also assume mobility ratio n/p=5/2, and the all logical efforts of the DFF and all loads are 1. The tCQ and setup/hold time are neglected. Find the critical delay of thefollowing circuit. (10%)



* + 1. The following figure shows the top view and section profile of a CMOS inverter. Fill in the remaining parts in upper-right and lower-left blocks. Remark the types (n, n+, p, p+) and terms (such as poly, thinox, diffusion, n-Well, PIMP, NIMP, M1, PO1…, etc.) at proper positions as complete as possible. (10%)



* + 1. Explain the following terms: (1) SoC (2) Active region (of a transistor) (3) FPGA (4) Wafer (5) Layout. (10%).