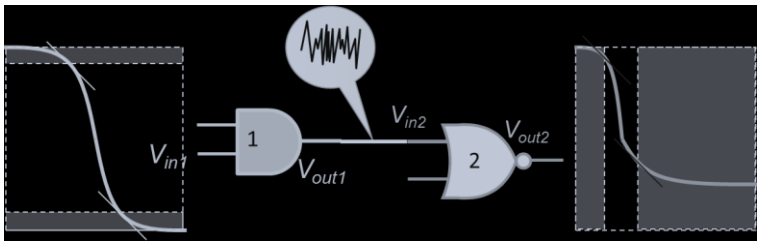
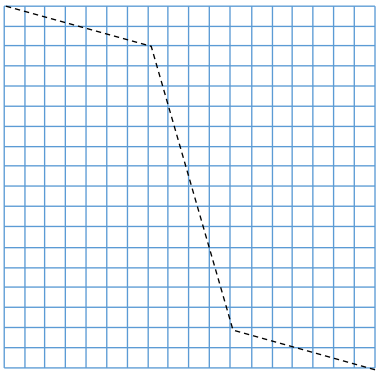
國立彰化師範大學電子系 109 學年第二學期隨堂考考卷

課目：VLSI 設計導論 日期：2021/3/17(Wed.) 時間：11:30~12:00am 地點：E406 老師：黃宗柱

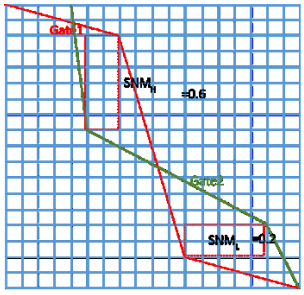
學號：_____ 姓名：_____ 得分：_____

Question 1: As the following figure, the characteristic curves of gates 1 and 2 are approximately PWL(0 1.8 0.7 1.6 1.1 0.2 1.8 0) and PWL(0 1.8 0.4 1.6 0.8 0.5 1.8 0.4) respectively. (a) Draw the butterfly diagram (20%), (b) Calculate the static noise margin (20%).





ANS:



Question 2: Draw the (a) schematics (15%), (b) N-path (10%), (c) P-path (10%) (d) stick diagram (20%) with a legend (5%) of Euler-path-oriented single-diffusion-line-based layout of the CMOS gate with $F = \overline{A(B+C+D)}$.