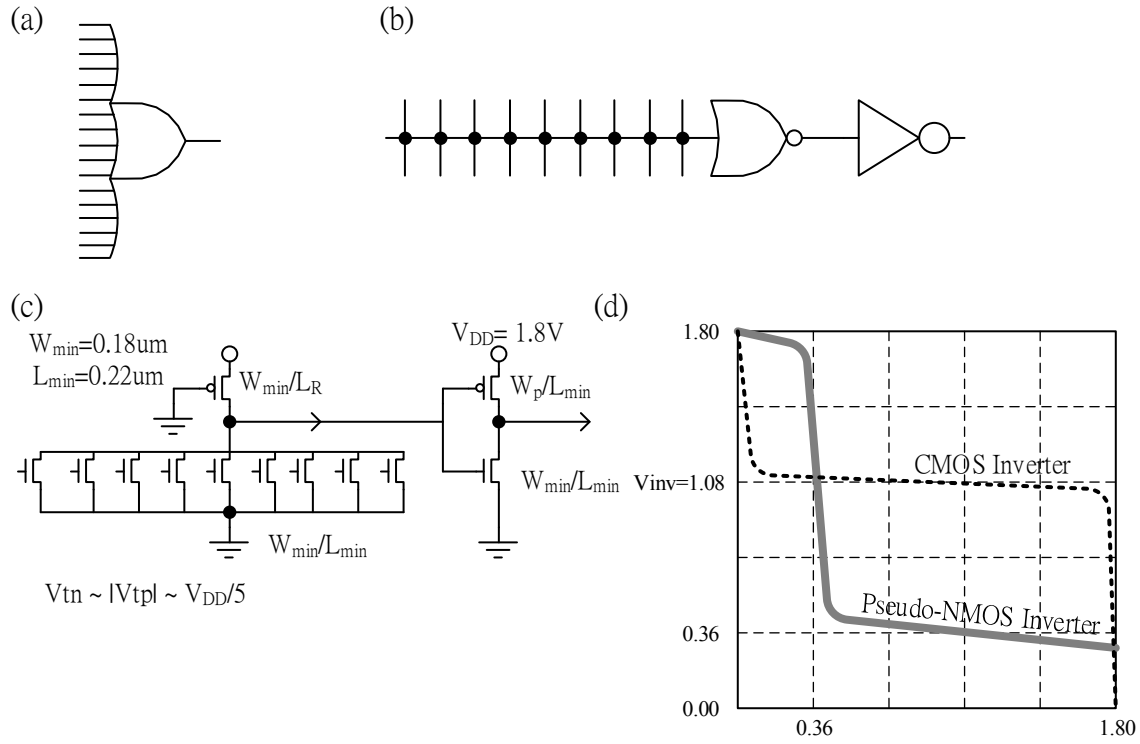
國立彰化師範大學電子系 109 學年第二學期隨堂考考卷

課目：VLSI 設計導論 日期：2021/5/5 (Wed.) 時間：08:30~09:00am 地點：E406 老師：黃宗柱

學號：_____ 姓名：_____ 得分：_____

As the following figures, (a) and (b) show symbols of many-input OR gates, and (c) shows the transistor-level design. Approximately a one-fifth (1:4) pull-on/off resistance is applied to design the pseudo-nMOS gate. The inversion voltage of the next CMOS inverter is then better to be turned up to $\frac{3}{5}V_{DD}$=1.08V. Decide the width L_R and the width W_p in μm.



Sol.

(1)

$\because$ Ron : Rp = 1:4, $L_R = \frac{4}{2.5}\ L_{min} = 0.288\mu m$

(2)

$\because I_{DS} = \frac{\beta_n}{2}(V_{inv} - V_{tn})^2 = \frac{\beta_p}{2}(V_{DD} - V_{inv} - |V_{tp}|)^2,\ S = \frac{2.5W_{min}}{W_p} = \frac{(5-3-1)^2}{(3-1)^2} = \frac{1}{4}$

$\therefore W_p = 2.5 \times 4 \times 0.18\mu m = 2.2\mu m$