國立彰化師範大學電子系 109 學年第二學期隨堂考考卷

課目：VLSI 設計導論 日期：2021/3/3(Wed.) 時間：08:30~09:00am 地點：E406 老師：黃宗柱

學號：_____ 姓名：_____ 得分：_____

Multiple Choice (單選題):

(A) 1. The thin oxide in CMOS technologies is usually manufactured by (A) Oxidation, (B) Deposition, (C) Diffusion, (D) Implantation.

(B) 2. The publishing of a wafer is usually done by (A) SOP, (B) CMP, (C) PNP, (D) HIP.

(C) 3. A depletion layer is generated by (A) P-P, (B) N-N, (C) P-N (D) SOI junctions.

(D) 4. The mobility ratio of the p-type hole and the n-type electron is about (A) 3:1, (B) 1:3, (C) 2.5:1, (D) 1:2.5.

(C) 5. In the following which is NOT a function of a polysilicon layer in a CMOS technology? (A) Self-Alignment, (B) Interconnection, (C) logic gate, (D) transistor gate.

(B) 6. The IC is innovated in (A) 1946, (B) 1956, (C) 1966, (D) 1976.

(D) 7. The major element in a usual IC is (A) Oxide, (B) Germanium, (C) Nitride, (D) Silicon.

(C) 8. The institute in Taiwan responsible for academic MPW projects is (A) MOSIS (SIS), (B) ITRI, (C) TSRI (CIC), (D) MOST (NSC).

(C) 9. The largest IC manufacture company is (A) SAMSUMG, (B) INTEL, (C) TSMC, (D) ASE.

(A) 10. The closest term to the foundry is (A) FAB, (B) Fabless, (C) Design, (D) Test.

請公正評分，改卷者簽字：_____