VLSI Design

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Brief Syllabus

1. Visit http://testlab.ncue.edu.tw/tch for details
2. Reference: Weste & Harris's textbook
3. All-English Instruction
4. Requirements for This Course:
   - ✓ Basic Logic Design
   - ✓ Hardware Descriptive Language
   - ✓ Self-Motivation
5. Addendum:
   - ✓ ftp://testlab.ncue.edu.tw/VLSI

Course Scope

1. Scoped in CMOS with 80% Digital + 20% Else
2. Why Go CMOS:
   1. Low power/cost
   2. High density
   3. High Noise Margin
   4. High Regularization
   5. Ratioless Circuits
   6. Compromised for Analog Design
   7. Highly Developed.
3. Why Digital First:
   1. High digitalization except AD/DA and a part of PLL
   2. Easy to start up

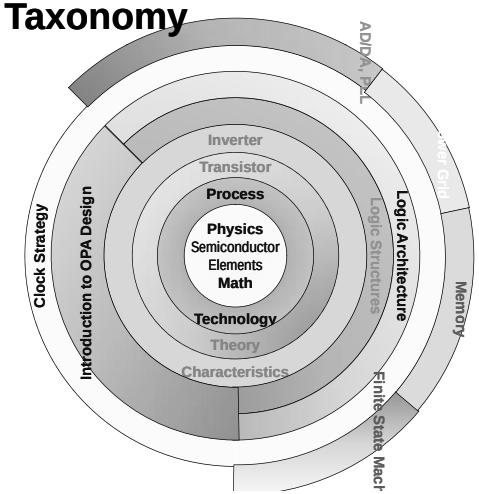
Major Contents

1. **Logic-Oriented MOS Theory – Transistor Sizing**
2. **Logic Cells – Full-custom Layout**
3. **Digital IC Synthesis – Cell-base Layout**
4. **Logic Structures and RTL Modules**
5. **Introduction to Digital IP**
6. **Introduction to Memory Design**
7. **Introduction to Logic Testing**
8. **Introduction to Some Basics for Analog Circuits**
9. **Introduction to SOC Design**

Today's Outline

- **Chips Everywhere! How do they come from?**
- **The IC Design Service in Taiwan, CIC**
- **Introduction to TSMC, the largest foundry**
- **Other FABs over the world**
- **Process Technology**
  - ➢ **Context Extracted from the above videos**
  - ➢ **Animation in the view of Layout Engineers**
- **Tapin Flow via CIC**
- **Homework #1 Given and due to 10/3.**

Field Taxonomy

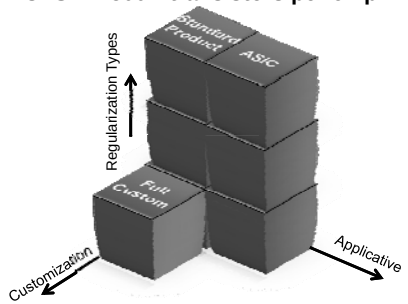


IC Evolution

- ✓ **1947 First Transistor (Shockley, Bardeen and Bratain)**
- ✓ **1958 TI Monolithic IC**
- ✓ **1959 Fairchild & TI Planar silicon IC**
- ✓ **1961 Fairchild & TI Commercial monolithic IC (RTL)**
- ✓ **1962 TI Diode-transistor logic (DTL)**
- ✓ **1962 Sylvania Transistor-transistor logic (TTL)**
- ✓ **1962 Motorola Emitter-coupled logic (ECL)**
- ✓ **1962 RCA & Fairchild MOS IC**
- ✓ **1963 RCA Complementary MOS (CMOS)**
- ✓ **1964 Fairchild First linear IC**
- ✓ **1968 Intel MOS memory chips**
- ✓ **1969 Bell Labs Charge-coupled devices (CCD)**
- ✓ **1970 Mostek MOS calculator chips**
- ✓ **1971 Intel Microprocessor**
- ✓ **1972 IBM & Philips Integrated Injection logic**

IC Evolution

✓ **1960-1966**	**SSI**	**~ 10 transistors per chip**
✓ **1966-1971**	**MSI**	**100 ~ 1000 transistors per chip**
✓ **1971-1980**	**LSI**	**1k ~ 20K transistors per chip**
✓ **1980-1985**	**VLSI**	**20k ~ 500K transistors per chip**
✓ **1985-**	**ULSI**	**> 500K transistors per chip**

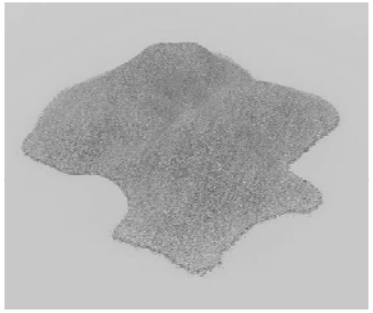


Chips Everywhere Now!

How is a CPU made?

Intel®01

- *from* **Sand**!
- 25% Si + O

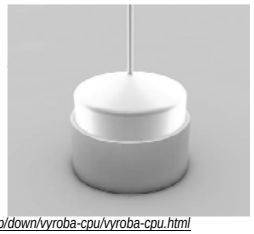


Refer to http://poli.cs.vsb.cz/edu/arp/down/vyroba-cpu/vyroba-cpu.html

Purification and Growing

Intel®01

- The silicon from sand is purified in multiple steps to finally reach semiconductor manufacturing quality to 1ppm alien atoms of **dopant**.
- In this picture you can see how one big crystal is grown from the purified silicon melt.
- The resulting mono-crystal is called an **ingot**.

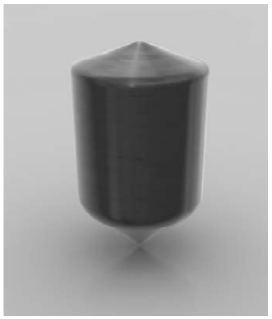


Refer to http://poli.cs.vsb.cz/edu/arp/down/vyroba-cpu/vyroba-cpu.html

Silicon Ingot

Intel®01

- One ingot weighs approximately 100 kg with a silicon purity of 99.9999 percent.
- Some ingots can stand higher than five feet (150cm).

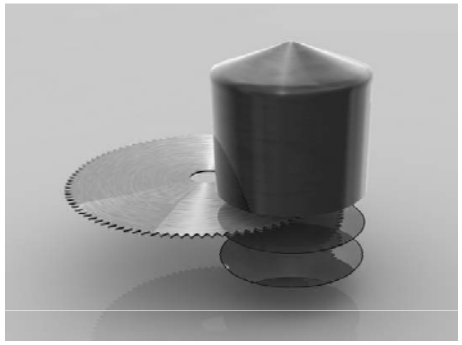


Refer to http://poli.cs.vsb.cz/edu/arp/down/vyroba-cpu/vyroba-cpu.html

Ingot Slicing

Intel®01

- The Ingot is then sliced to **wafers**.
- Today, CPUs are commonly made on 300 mm (12") wafers.

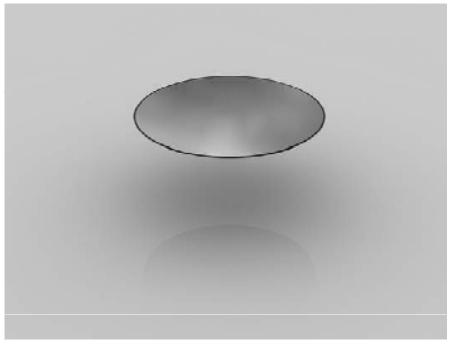


Refer to http://poli.cs.vsb.cz/edu/arp/down/vyroba-cpu/vyroba-cpu.html

Lapping and Publishing

Intel®01

- After slicing the wafers are lapped and polished until they have flawless, mirror-smooth surfaces.

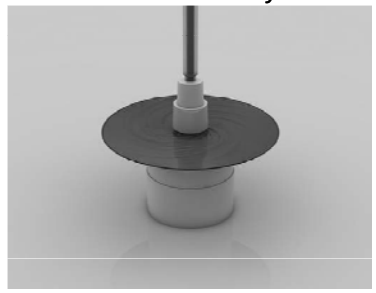


Refer to http://poli.cs.vsb.cz/edu/arp/down/vyroba-cpu/vyroba-cpu.html

Photo Resist Application

Intel®01

- The blue liquid is a photo resist (PR) finish similar to those used in film for photography.
- The wafer spins during this step to allow an evenly-distributed coating that's smooth and also very thin.
- The photograph is analogy to traditional lithography.

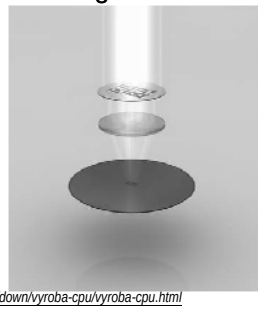


Refer to http://poli.cs.vsb.cz/edu/arp/down/vyroba-cpu/vyroba-cpu.html

UV Light Exposure

Intel®01

- PR finish is exposed to ultra violet (UV) light.
- For +film, exposed area will become soluble, and vice versa.
- Using masks that act like stencils creating various circuit patterns.
- A lens reduces the mask's image to a small focal point.
- The resulting "print" on the wafer is typically 4X smaller, than the mask's pattern.

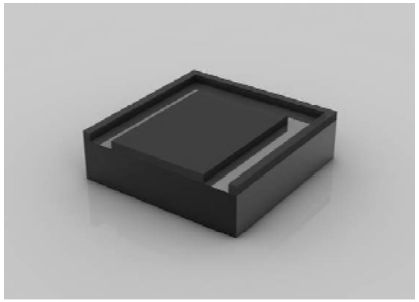


Refer to http://poli.cs.vsb.cz/edu/arp/down/vyroba-cpu/vyroba-cpu.html

PR Washing

Intel®01

- The PR is completely dissolved by a solvent. This reveals a pattern of photo resist made by the mask.

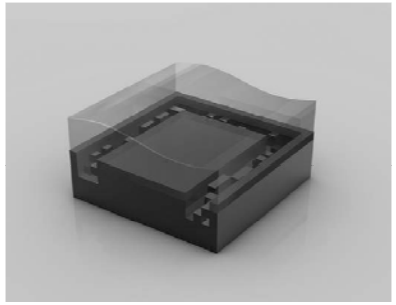


Refer to http://poli.cs.vsb.cz/edu/arp/down/vyroba-cpu/vyroba-cpu.html

Etching

Intel®01

- The photo resist layer protects wafer material that should not be etched away.
- Areas that were exposed will be etched away with chemicals.

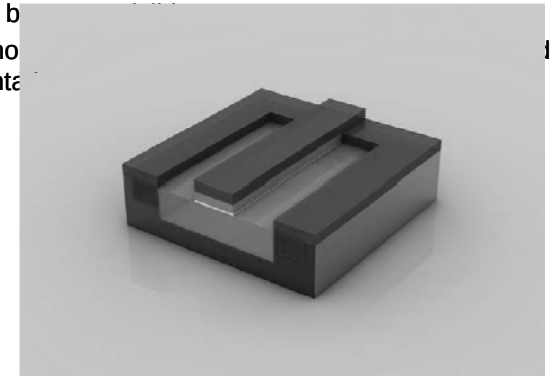


Refer to http://poli.cs.vsb.cz/edu/arp/down/vyroba-cpu/vyroba-cpu.html

Iron Doping

Intel®01

- After etching the PR is removed and the desired shape b
- Commo
  implanta

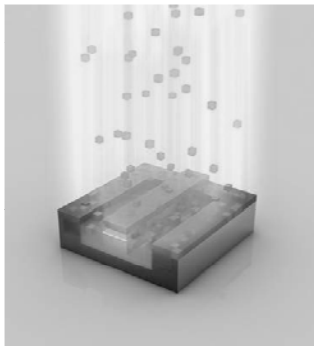


Refer to http://poli.cs.vsb.cz/edu/arp/down/vyroba-cpu/vyroba-cpu.html

Iron Implantation

Intel®01

- The exposed areas of the silicon wafer are bombarded with ions.
- Ions are implanted in the silicon wafer to alter the way silicon in these areas conduct electricity.
- Ions are propelled onto the surface of the wafer at very high velocities ~ 10^5m/s.



Refer to http://poli.cs.vsb.cz/edu/arp/down/vyroba-cpu/vyroba-cpu.html

Wafer Electroplating

Intel®01

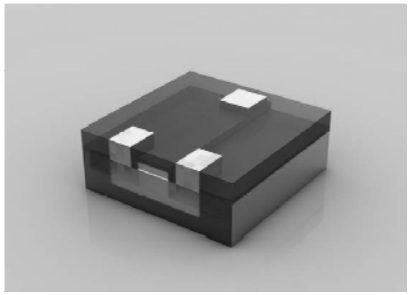
- The wafers are put into a copper sulphate solution at this stage.
- Copper ions are deposited onto the transistor through a process called electroplating.
- The copper ions travel from the positive terminal (anode) to the negative terminal (cathode) which is represented by the wafer.
- Then the copper ions settle as a thin layer on the wafer surface.

Refer to http://poli.cs.vsb.cz/edu/arp/down/vyroba-cpu/vyroba-cpu.html

Iron-Settle Polishing

Intel®01

- The excess material is polished off leaving a very thin layer of copper.

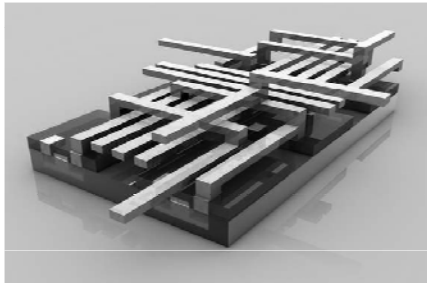


Refer to http://poli.cs.vsb.cz/edu/arp/down/vyroba-cpu/vyroba-cpu.html

Layering

Intel®01

- Multiple metal layers are created to interconnects in between transistors.
- While computer chips look extremely flat, they may actually have over 20 layers to form complex circuitry.

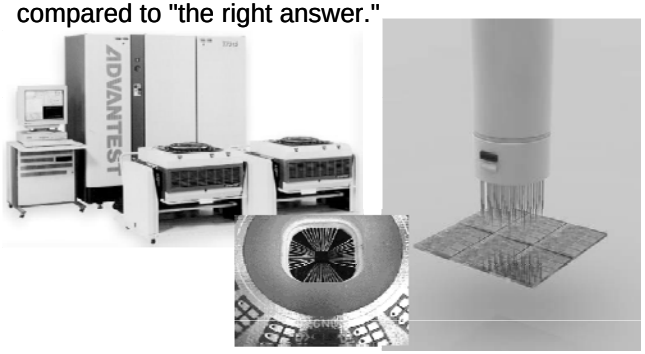


Refer to http://poli.cs.vsb.cz/edu/arp/down/vyroba-cpu/vyroba-cpu.html

Wafer Testing

Intel®01

- In this stage test patterns are fed into every single chip and the response from the chip monitored and compared to "the right answer."

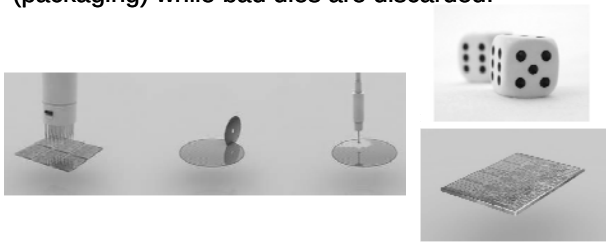


Refer to http://poli.cs.vsb.cz/edu/arp/down/vyroba-cpu/vyroba-cpu.html

Die Screening

Intel®01

- The chips are inked into good, ugly and bad dies by wafer testing.
- Then the dies are sliced.
- Good dies will be put forward for the next step (packaging) while bad dies are discarded.

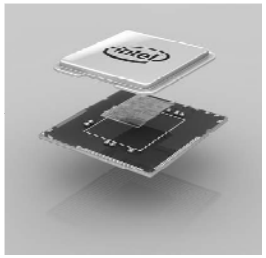


Refer to http://poli.cs.vsb.cz/edu/arp/down/vyroba-cpu/vyroba-cpu.html

IC Packaging

Intel®01

- The substrate, the die, and the heatspreader are put together to form a completed processor.
- The green substrate builds the electrical and mechanical interface for the processor to interact with the rest of the PC system.
- The silver heatspreader is a thermal interface where a cooling solution will be applied.



Refer to http://poli.cs.vsb.cz/edu/arp/down/vyroba-cpu/vyroba-cpu.html

Final Test: CPU Testing

Intel®01

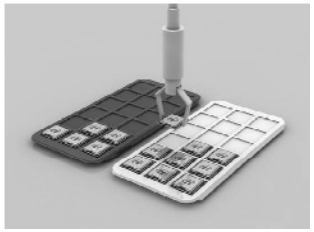
- During final test the processors are tested for their key characteristics, usually the tested characteristics are power dissipation and maximum frequency.

Refer to http://poli.cs.vsb.cz/edu/arp/down/vyroba-cpu/vyroba-cpu.html

IC Binning and Grading

Intel® 01

- Based on the test result of class testing processors with the same capabilities are put into the same transporting trays.
- This process is called "binning," a process with which many *Tom's Hardware* readers will be familiar.
- Binning determines the maximum operating frequency of a processor, and batches are divided and sold according to stable specifications.



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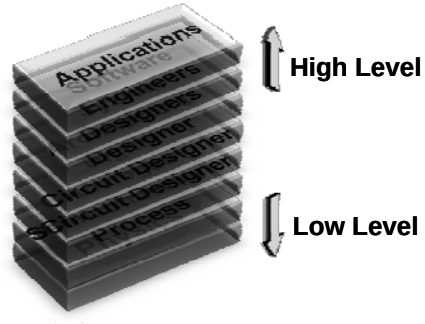
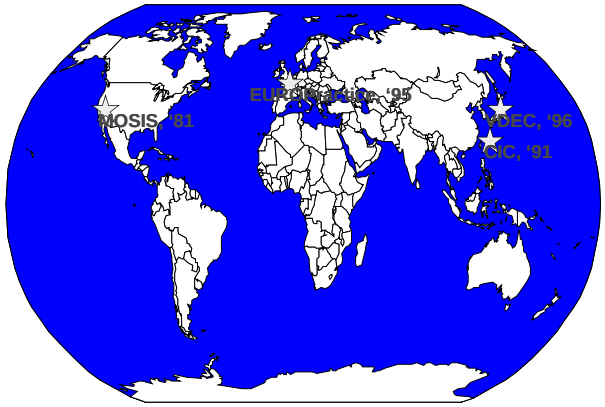
The IC-Design Building



Some Terminology

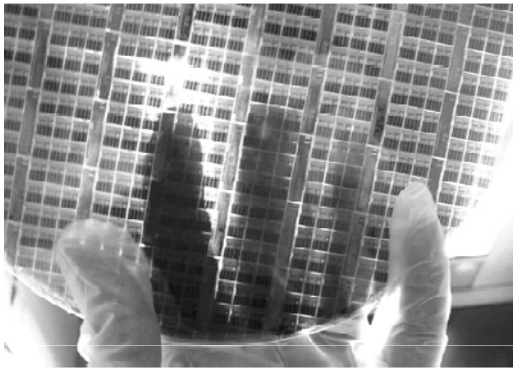
- FAB: fabrication, analogy to layout-style manufacture
- Foundry: factory for basing the industry chain like the metal castings, especially for semiconductor industry
- FABless Design House: small design company usually w/o FAB equipments
- CIC: Chip Implementation Center, National Applied Research Laboratories
- MPW: Multi-Project Wafer

IC FAB MPW Services



Refer to http://www.cic.org.tw

Some Videos on Semiconductor Wafer Process



Videos on Silicon Wafer Processing

- Wafer Process at Texas Instrument, 2000 (9 min)
- Semiconductor Technology at TSMC, 2011 (8 min)
- Chip Manufacture Process, 2008 (10min)
- CPU Manufacture at AMD, 2009 (11min)
- Intel 22nm FinFET Process Flow, 2013 (10min)

Context Reviews on Process Tech

1. Si Semiconductor Technology
2. Basic CMOS Technology
3. CMOS Process
4. Layout Design Rules
5. Latchup Effect
6. Extractor & DRC
7. An n-Well CMOS Process Flow
8. CIC Tape-In Flow & Tutorial

CMOS Process Tech

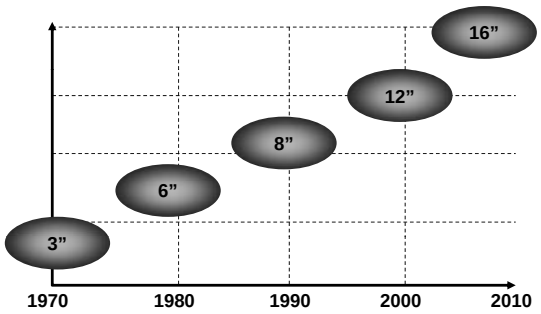
1. **Oxidation** (氧化)
2. **Epitaxy** (磊晶)
3. **Deposition** (沉積)
4. **Implantation** (植入)
5. **Diffusion** (擴散)

Ingot Production

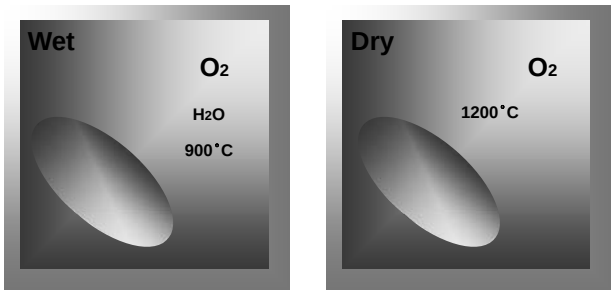
Wafer Treatments

1. **Grinding** delete coarse surface by crushing
2. **Slicing** separate to wafers
3. **Lapping** flatten by press
4. **Etching** delete by dissolving
5. **Polishing** flatten fine as a mirror
6. **Cleaning**
7. **Inspection** probably by peer eyes

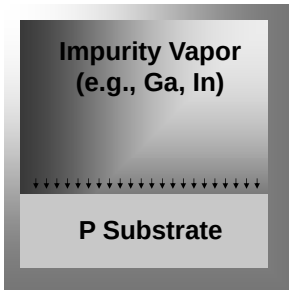
Wafer Size



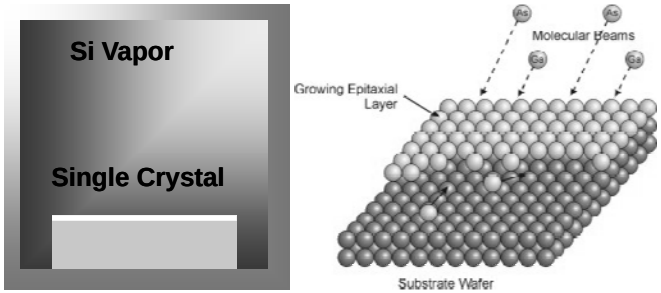
Oxidation



Chemical Vapor Deposition

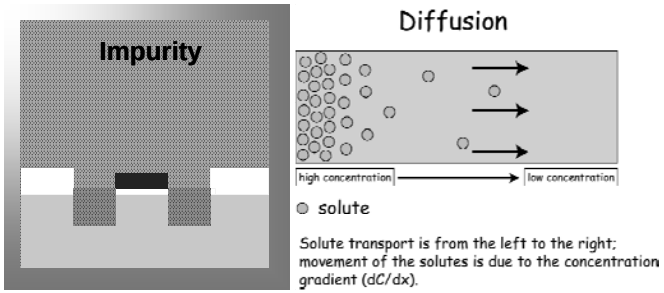


Epitaxy

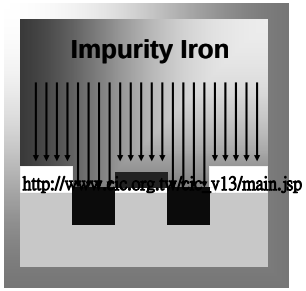


MBE

Diffusion

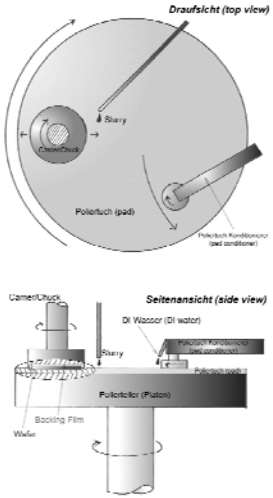


Iron Implantation

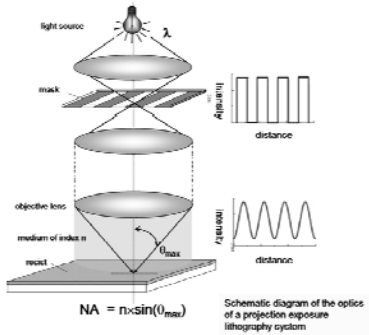


1. **Previously used to adjust the threshold voltage;**
2. **Currently usually used to be active region.**

Chemical Mechanical Polishing (CMP)



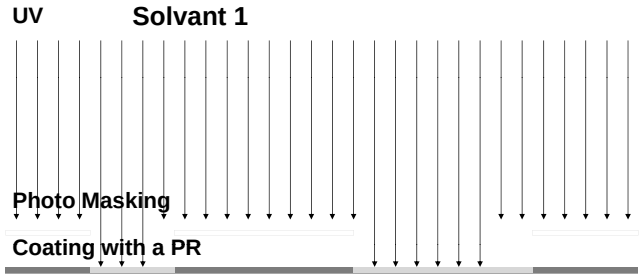
Lithography



Common Material Used As Masks

1. Photoresist
2. Polysilicon
3. Silicon Dioxide
4. Silicon Nitride

Masking using PR



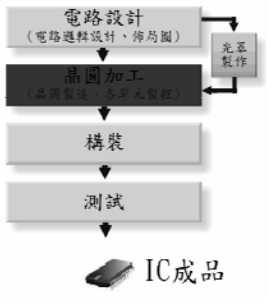
Sloved after the process using the mask (eg. negative film)

Self-Align: if the rest mask is also a useful layer.

Basic CMOS Technology

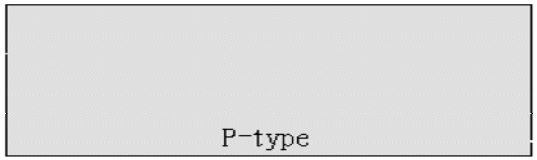
1. N-Well Process
2. P-Well Process
3. Twin-Well (Twin-Tub) Process
4. Silicon on Insulator

Major IC Manufacture Flow



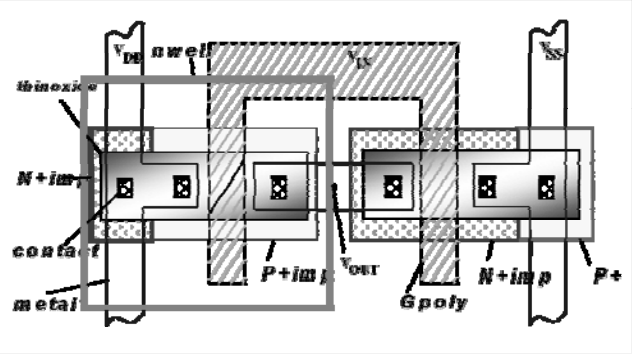
- IC design
- Wafer fabrication, FAB
- Packaging
- Test

A Detailed MOS Process



Courtesy of Chuang, "VLSI Technology," ISBN:957-584-327-4 .

A NOT Gate (An Inverter)

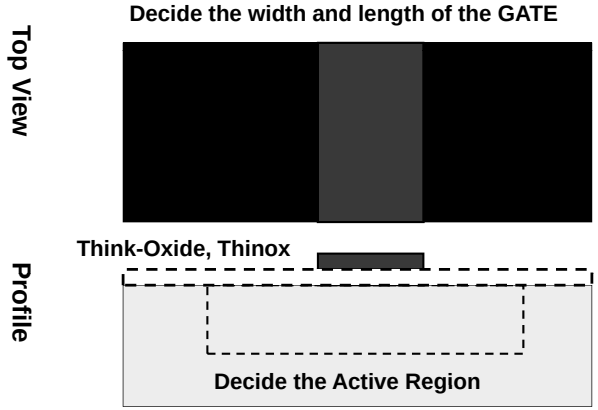


Homework #1

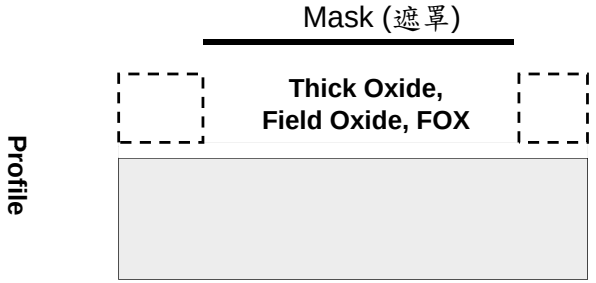
- Download the homework sheet from the website. Try to answer the problem in English. Due 2011/10/03.

1. Draw the intersection profile of the top-down view of the inverter in last page (50). Denote each materials by m1, n, p, n+, p+, poly, thinox, substrate and n-well for metal1, n/p-type etc.
2. Why can the MPW save the manufacturing cost for students?
3. Explain the following terminology: latchup effect, CVD, CMP, TSMC, Foundry, CIC, Self-Align Effect, PR, Active Region and Electron Mobility.

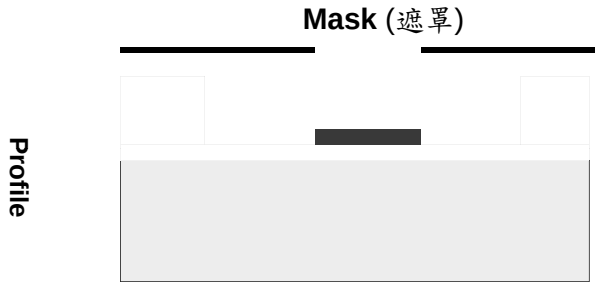
Simplified Layout of a Transistor



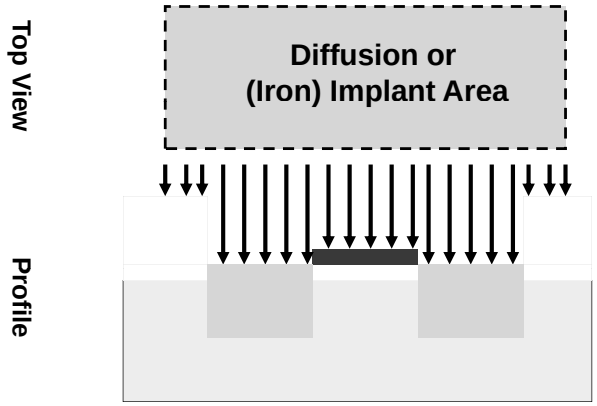
Simplified Layout of a Transistor



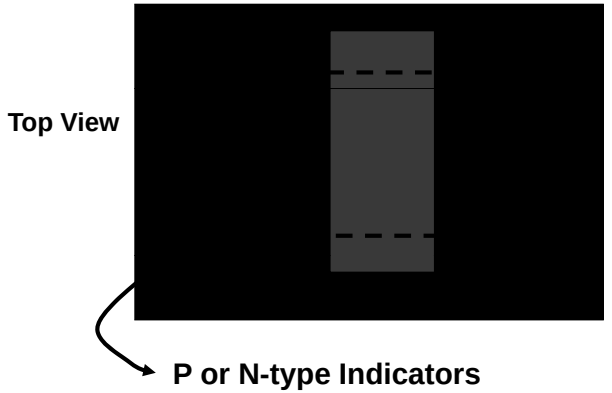
Simplified Layout of a Transistor



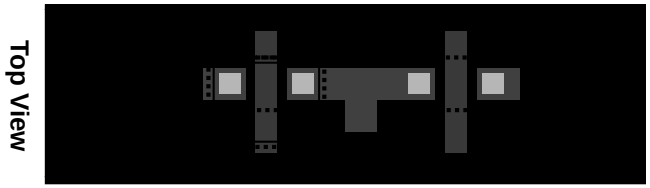
Simplified Layout of a Transistor



Simplified Layout of a Transistor



W/L Ratio due to the Mobility



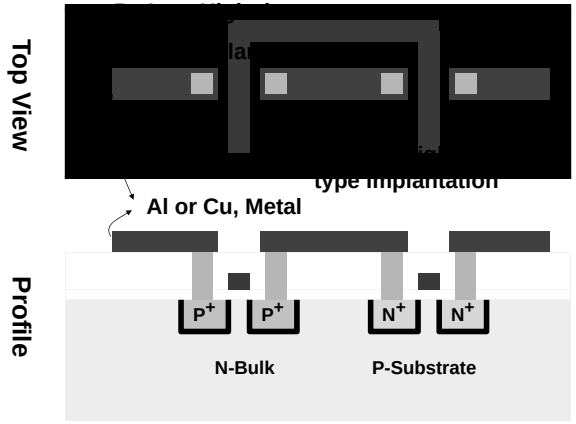
P-type Transistor N-type Transistor

Because of Electron Mobility, μ ~ 1 : 2.6

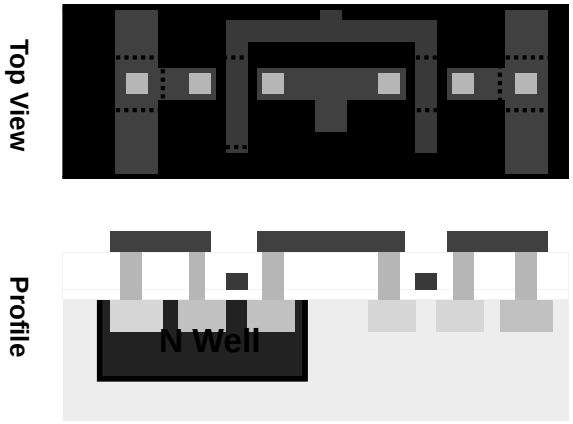
Usually for balancing Noise Margin and then inversion voltage

W/L of P-type transistor is 2-3 folds of N-type

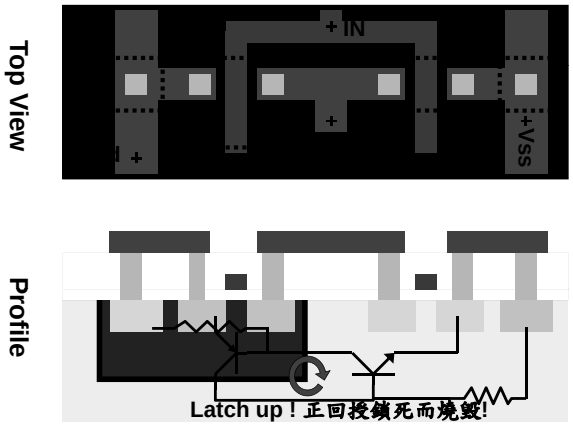
N-Well Process Technology



N-Well Process Technology



Latch-up Effect in n-Well Process



Preventing Latch-up

1. Using Twin-Well
2. Evolved in DRC
   - Connect N/P-well to Vdd/Vss
   - Contacts closer to Source-gate
   - More contacts for more transistors
   - Sometimes one well contact for a transistor.

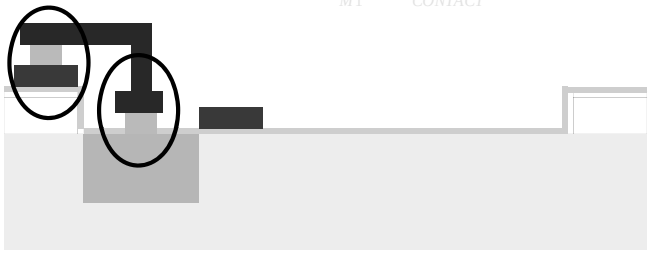
Contact

Basic 4 Layers:

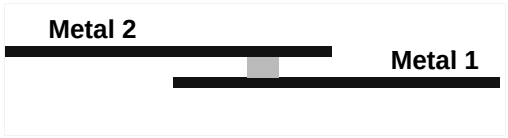
$W_{DIFFUSION} > W_{CONTACT}$

$W_{THINOX} > W_{CONTACT}$

$W_{M1} > W_{CONTACT}$



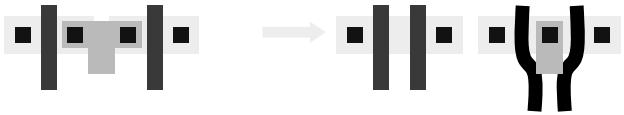
Via



The widths of a via or contact are much sensitive to the process so that they are usually optimized to a constant, say 0.4um in 0.35um technology.

Local Interconnections

Diffusion as interconnection:



1. **Diffusion: < 1 Transistor**
2. **N-Well: < 1~5 Transistors**
3. **Polysilicon: 1~5 Transistors**

SAlicide

Polysilicon Process

Polysilicon: a multi-crystal semiconductor, Rs~10

Silicide Process

Silicide: a refractory metal, e.g., Si+Ta, Rs~1

Polycide Process

Self-Aligned Polycide Process

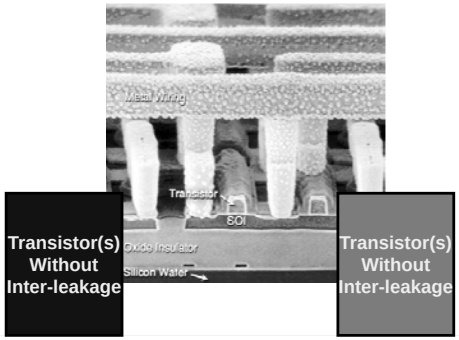
Thin Film Process

SOI Process

Thin Film Transistor (TFT)

Hi-density memory, Flat-Panel Display

Silicon on Insulator (SOI)



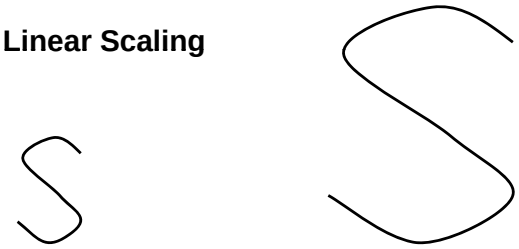
Sapphire (藍寶石) or Glass

Design Rule Check (DRC)

1. **Geometrical**
   - **X-Y Plane: Single-Layer Layout**
   - **Z Plane: Interactions btw Layers**
2. **ERC**
   - **Electrical Rule Check**
3. **Custom Rules**

Scaling

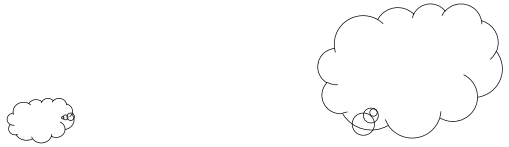
1. **Linear Scaling**



$C=K$ $\quad C=\lambda K$

Scaling

2. **First Order Scaling**

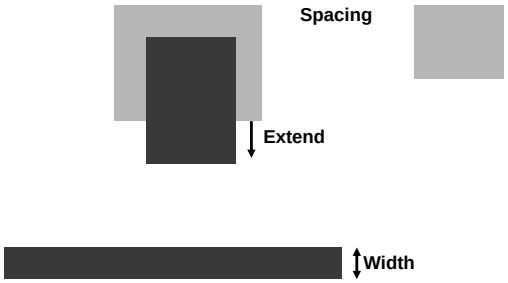


$A=K$ $\quad A=\lambda^2 K$

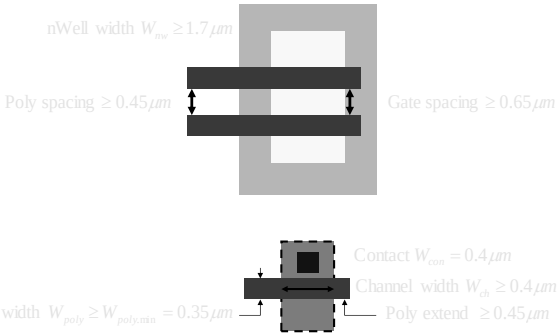
Basic Categories of Rules

1. **Micron (μ) Rules**
   - **Listing all min. feature sizes in μ's**
   - **Re-listing is required after scaling.**
2. **Lambda (λ) Rules**
   - **The min. active width = 1 λ (μm).**
   - **Linear Scaling by λ (λ/μ Rule).**
   - **First Order Scaling.**
   - **Must be modified in another range.**

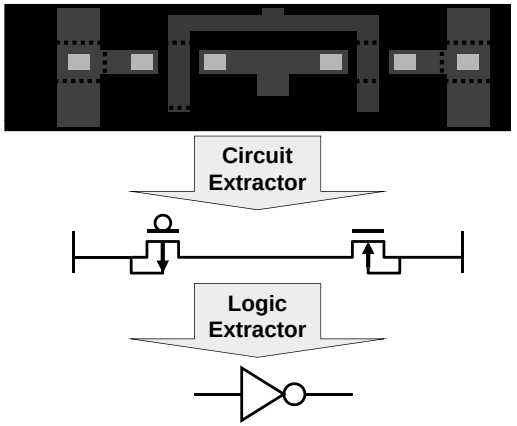
Basic Parameters in DRC



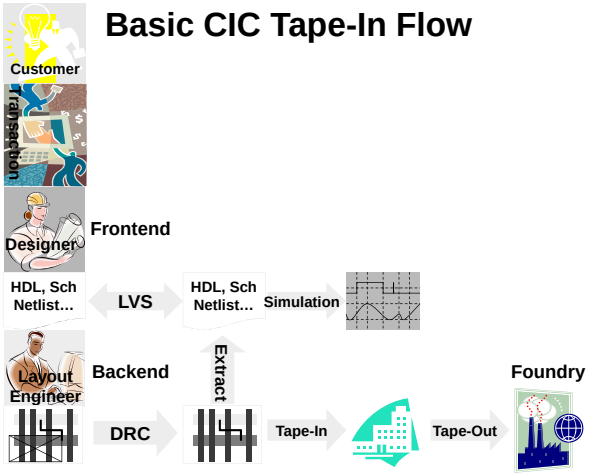
Some Rules in TSMC.35-2P4M(P)



Some Related Terminology



Basic CIC Tape-In Flow



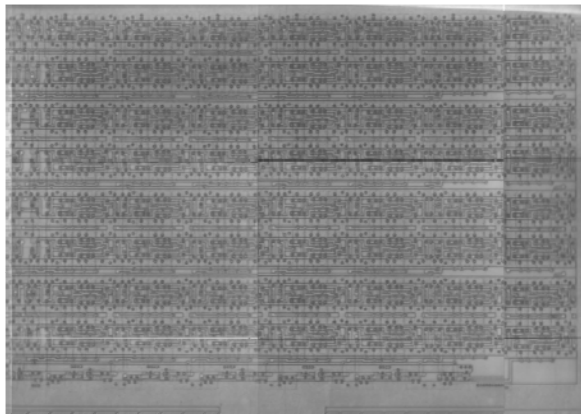
Reverse Engineering (RE)

1. Category
   - Mechanism
   - Software: database, programming
   - VLSI: layout
2. Purpose:
   - Failure inspection
   - Amoral hack, referring
   - Illegal stealing (duplication)

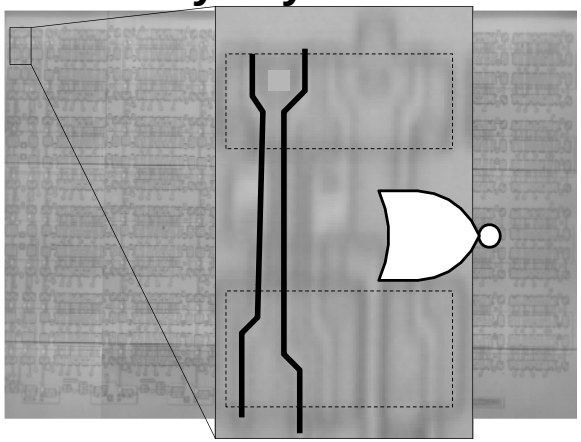
VLSI RE Flow

1. Unpacking
2. Chemical Metal Polishing (CMP)
3. Photographing
4. Inspection
5. Schematic
6. Simulation & Verification

A Metal Layer Photo

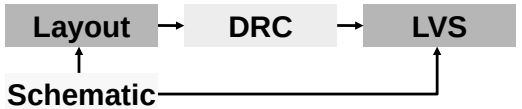


A Poly Layer Photo



Reversing Rule Check

Forward Engineering:



Reverse Engineering: