**Final Examination Sheet**

Spring Semester, 2021, Dept. of Electronics Eng., National Changhua Univ. of Edu.

Course：***Introduction to VLSI Design*** Date：2021/6/23 (Wed.) Time：09:20~11:00 Online Exam.

***Note***: You can answer your exam by one of the following steps:

1. Please full-in or paste your answer by drafting using PowerPoint or Excel, transfer to pdf, name the file using your Reg.No and email to tch@cc.ncue.edu.tw by 11:20am.
2. Otherwise, you can write down your answers on paper and have a picture by camera, (paste them to a winword file, transfer to pdf), name the file using your Reg.No, and then email to tch@cc.ncue.edu.tw.

Reg. No.：\_\_\_\_\_\_\_\_\_\_\_\_\_\_ Student’s Name：\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

1. TRUE OR FALSE (Mark ○ or X, 20%):

( ) 1. SKILL is a scripting language which can be applied in Virtuoso for full-custom layout.

( ) 2. “module m(C, I, O); input C, I; reg O; always@(posedge C) O=I; endmodule” can be correctly compiled in Verilog.

( ) 3. An 8-bit adder is verified if the output is 20 for inputs 13 and 7.

( ) 4. It is called technology mapping to implement Boolean functions into specific logic cells.

( ) 5. EDA Scripting is to take general or tool command language interpreters to automate 1 electronic design packages.

( ) 6. The rule of tens approximately explains the decision whether to test or not in each manufacturing stages.

( ) 7. Usually a 16GB NOR type Flash SD is more expensive than the a 32GB NAND type Flash memory stick.

( ) 8. The increment c++ in C language takes about one half of gate count and one half of carry propagation time.

( ) 9. 0-1 march test detects more faults than.

( ) 10. IC test can be fully saved if a fault tolerant mechanism is built in.

1. MULTIPLE CHOICE (Choose the best one, 20%):

( ) 1. Which is not a purpose of growing poly-silicon prior to iron implementation, (A) serving as a mask (B) preventing from latchup (C) working as a transistor gate (D) self-alignment.

( ) 2. In a high-voltage layout which is usually enhanced? (A) thinox thickness (B) gate extension (C) transistor pitch (D) drain distance.

( ) 3. A recent global problem is the shortage of (A) water (B) automotive chips (C) labor (D) capital.

( ) 4. Which control signal provides a short and constant-width pulse? (A) Reset (B) Clock (C) Toggle (D) Strobe.

( ) 5. Which type of logic structure usually takes low power and long time? (A) AOI (B) OAI (C) NOR (D) NAND.

( ) 6. Which diagram shows the working boundaries of products? (A) I-V (B) Space-Time (C) Shmoo (D) ladder diagram.

( ) 7. Which is mainly responsible for transistor-level simulation? (A) Encounter (B) Debussy (C) HSPICE (D) Virtuoso.

( ) 8. Owing to clock wire resistance, shift registers overpass in a cycle is caused by (A) transparent output (B) setup time violation (C) hold time violation (D) bus contention.

( ) 9. Voltage-dividing effect of an SRAM cell tends to occur at its (A) write (B) standby (C) read (D) search mode.

( ) 10. Which adder is usually designed for many inputs? (A) carry skip (B) carry select (C) carry save (D) carry ripple.

1. QUESTIONS (120%, at most 60% adopted):
2. As the following figure, the peak-to-peak jitter and skew is defined as the maximum *tC1C2* = *tJ*. Clock-to-Q times *tCQ* of successive flip-flops FF1 and FF2 are given. The critical path of the combinational circuit takes a *tp* propagation time. Hold time *tH* and setup time *tS* are constraint constant time for flip-flops. Derive the setup-time and hold-time rules in two inequations according to the following figure. (20%)



1. Draw a typical diagram of a RAM array according to the lecture. (15%) (including row/col address decoders, SA, WLs, BLs, controller, SRAM cells, etc.)
2. In the following figure, PLL*i* means the *i*-th ideal phase lock loop to provide clock source of domain i with an average skew . To reduce the relative skew of all domains, a delay line with delay is applied to beed back loop. Explain the operations and calculate the relation between and domain average skews. (15%)



1. A multiplier cell is given. Draw a parallel multiplier with cells. The input/output paths drawn in dashed lines and the carry paths solid lines. (15%)



1. Using a typical FSM design procedure, design a 1-input 1-output sequence detector that will outputs 1 only when it receives a sequence 1111. Implement the FSM by programming (burn on with a notation X) on the following PLA diagram (with AND and OR arrays). (20%)



1. Given the fault list of the following circuit as L*f* = {A0, A1, B0, B1, C0, C1, F0, F1, G0, G1, H0, H1} where Gx means gate G stuck-at-x fault, (1) justify and propagate to find the test pattern TG0 of G0. (2) Then do deductive fault simulation to collect all testable faults of TG0. (3) Calculate the fault coverage of TG0, FC(TG0, L*f*). (20%)





* + 1. Assume F is a 3-input function, , map and program F into the following different structures. Write the bitstream for programming the LUT. (15%)

