**Samples and Reviews for Final Examination**

**Fill-in or Paste your Answer, Transfer to PDF and Email to me (tch@cc.ncue.edu.tw) by June 23, 11:30am**

Course：***Introduction to VLSI Design*** Date： Time：09:30~11:00 Place：Online

Reg. No.：\_\_\_\_\_\_\_\_\_\_\_\_\_\_ Student’s Name：\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ Grade：\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

1. TRUE OR FALSE (Mark ○ or X, 20%):

( ) 1. The increment c++ in C language takes about one half of gate count and one half of carry propagation time.

( ) 2. 0-1 march test detects more faults than.

( ) 3. The rule of tens approximately explains the decision whether to test or not in each manufacturing stages.

( ) 4. Usually a 16GB NOR type Flash SD is cheaper the a 32GB NAND type Flash memory stick.

( ) 5. IC test can be fully saved if a fault tolerant mechanism is built in.

( ) 6. The smallest oscillator can be implemented by connecting the output of a CMOS inverter to its input.

( ) 7. “module m(C, I, O); input C, I; reg O; always@(posedge C) O=I; endmodule” can be correctly compiled in Verilog.

( ) 8. An 8-bit adder is verified if the output is 20 for inputs 13 and 7.

( ) 9. It is called technology mapping to implement Boolean functions into specific logic cells.

( ) 10. EDA Scripting is to take $\geq 1$ general or tool command language interpreters to automate $\geq $ 1 electronic design packages.

1. MULTIPLE CHOICE (Choose the best one, 20%):

( ) 1. Voltage-dividing effect of an SRAM cell occurs at its (A) write (B) standby (C) read (D) search mode.

( ) 2. Which power dissipation is most sensitive to the supply voltage? (A) static current (B) dynamic power (C) short current (D) subthreshold current.

( ) 3. CMRR mainly comes from (A) current mirror (B) accumulator (C) differential pair (D) compensation.

( ) 4. Which is not a purpose of growing poly-silicon prior to iron implementation, (A) serving as a mask (B) preventing from latchup (C) working as a transistor gate (D) self-alignment.

( ) 5. In a high-voltage layout which is usually enhanced? (A) thinox thickness (B) gate extension (C) transistor pitch (D) drain distance.

( ) 6. Which is mainly responsible for transistor-level simulation? (A) Encounter (B) Debussy (C) HSPICE (D) Virtuoso.

( ) 7. Owing to clock wire resistance, shift registers overpass in a cycle is caused by (A) transparent output (B) setup time violation (C) hold time violation (D) bus contention.

( ) 8. Which is to control the transition of contiguous states is an FSM? (A) Reset (B) Clock (C) Toggle (D) Strobe.

( ) 9. Which type of logic structure usually takes low power and long time? (A) AOI (B) OAI (C) NOR (D) NAND.

( ) 10. Which diagram shows the working boundaries of products? (A) I-V (B) Space-Time (C) Shmoo (D) ladder diagram.

1. QUESTIONS (120%, at most 60% adopted):
2. As the following figure, the peak-to-peak jitter and skew is defined as the maximum *tC1C2* = *tJ*. Clock-to-Q times *tCQ* of successive flip-flops FF1 and FF2 are given. The critical path of the combinational circuit takes a *tp* propagation time. Hold time *tH* and setup time *tS* are constraint constant time for flip-flops. Derive the setup-time and hold-time rules in two inequations according to the following figure. (20%)



1. Draw a typical diagram of a RAM array according to the lecture. (15%) (including row/col address decoders, SA, WLs, BLs, controller, SRAM cells, etc.)
2. In the following figure, PLL*i* means the *i*-th ideal phase lock loop to provide clock source of domain i with an average skew $σ\_{i}$. To reduce the relative skew of all domains, a delay line with delay $Δt\_{i}$ is applied to beed back loop. Explain the operations and calculate the relation between $Δt\_{i}$ and domain average skews. (15%)



1. A multiplier cell is given. Draw a $4×4$ parallel multiplier with $4×4$ cells. The input/output paths drawn in dashed lines and the carry paths solid lines. (15%)



1. Using a typical FSM design procedure, design a toggle flip-flop TFF that receives an input T and toggles Q only when T is 1. Implement the FSM by programming (burn on with a notation X) on the following PLA diagram. (20%)



1. Given the fault list of the following circuit as L*f* = {A0, A1, B0, B1, C0, C1, F0, F1, G0, G1, H0, H1} where Gx means gate G stuck-at-x fault, (1) justify and propagate to find the test pattern TG1 of G1. (2) Then do deductive fault simulation to collect all testable faults of TG1. (3) Calculate the fault coverage of TG1, FC(TG1, L*f*). (20%)





* + 1. Assume F is a 3-input function, $F=AB+BC$, map and program F into the following different structures. Write the bitstream for programming the LUT. (15%)

