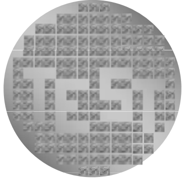

VLSI Test

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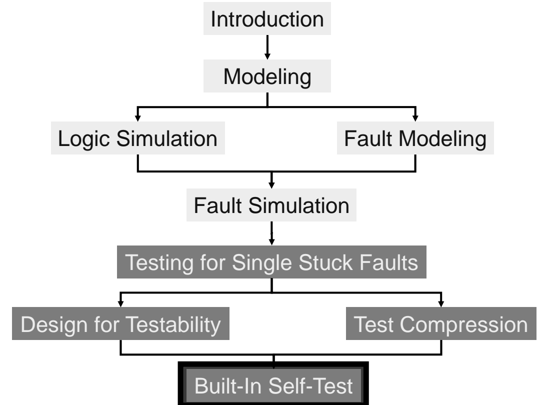
Syllabus & Chapter Precedence



Built-In Self-Test (BIST)
Objectives

1. To Reduce input/output pin signal traffic.
2. Permit easy circuit initialization and observation.
3. Eliminate as much test pattern generation as possible.
4. Achieve fair fault coverage on general class of failure mode.
5. Reduce test time.
6. Execute at-speed testing.
7. Test circuit during burn-in.

Built-In Self-Test (BIST)
Issues

1. Area overhead
2. Performance degradation
3. Fault coverage
4. Ease of Implementation
5. Capability for system test
6. Diagnosis capability

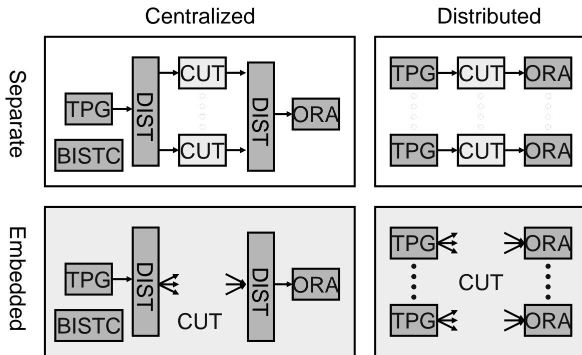
Typical BIST Techniques

1. Stored Vector Based (Pattern Generated)
   1. Microinstruction support
   2. Stored in ROM
2. Algorithmic Hardware Test Pattern Generators
   1. Counter
   2. Linear Feedback Shift Register
   3. Cellular Automata
   4. FSM (ASM) Based

Classification

1. Forms
   1. Off-Line
      - Functional
      - Structural
   2. On-Line
      - Concurrent
        - Parallel
        - Pipeline
        - Asynchronous
      - Non-concurrent
2. Level
   1. Production Testing
   2. Field Testing
3. TPG for BIST
   1. Exhaustive Testing
   2. Pseudo-random Testing
      - Weighted
      - Adaptive
   3. Pseudo-exhaustive Testing
      - Counter-Based: Syndrome, Constant-Weight
      - LFSR-Based: Shift/Scan, XOR, Condensed, Cyclic

General BIST Architecture



TPG: Test Pattern Generator, CUT: Circuit under Test, ORA: Output Result Analyzer, BISTC: BIST Controller

Specific BIST Architecture

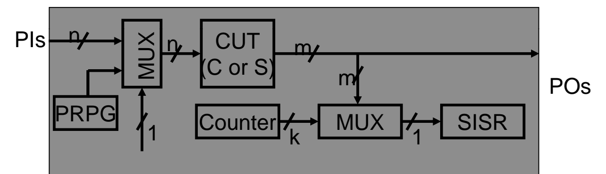
Architecture	Ref.	Remark
CSBL	Benowitz, 1975	Centralized & Separate Board-Level BIST
BEST	Resnick, 1983	Built-In Evaluation and Self-Test
RTS	Bardell, 1982	Random Test Socket
LOCST	Eichelberger, 1983	LSSD On-Chip Self-Test
STUMPS	Bardell, 1982	Self-Testing Using MISR and Parallel SRSG
CBIST	Saluja, 1988	Concurrent BIST
CEBS	Komanytsky, 1982	Centralized and Embedded BIST with Boundary Scan
RTD	Bardell, 1987	Random Test Data
SST	Gupta, 1982	Simultaneous Self-Test
CATS	Burkness, 1987	Cyclic Analysis Testing System
CSTP	Krasniewski, 1989	Circular Self-Test Path
BILBO	Koenemann, 1979	Built-In Logic-Block Observation

Specific BIST Architecture

Architecture	Ref.	Control	Circuit	On-line	Boundary	Scan
CSBL	Benowitz, 1975	Centralized	Separate	V		
BEST	Resnick, 1983	Centralized	Separate		V	
RTS	Bardell, 1982	Distributed	Separate		V	LSSD
LOCST	Eichelberger, 1983	Centralized	Separate		V	LSSD
STUMPS	Bardell, 1982	Centralized	Separate		V	Multiple
CBIST	Saluja, 1988	Centralized	Separate	V		
CEBS	Komanytsky, 1982	Centralized	Embedded		V	
RTD	Bardell, 1987	Distributed	Embedded			
SST	Gupta, 1982	Distributed	Embedded			No LFSR
CATS	Burkness, 1987	Centralized	Separate			
CSTP	Krasniewski, 1989	Centralized	Separate			
BILBO	Koenemann, 1979	Distributed	Embedded			

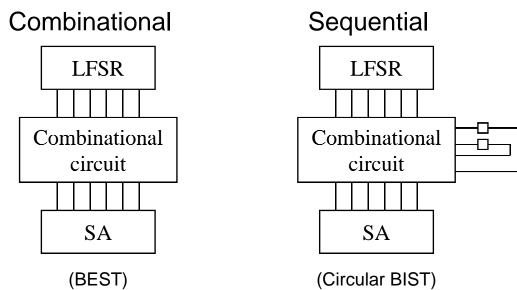
Specific BIST Architecture (1)

CSBL



1. Centralized and Separate Board-Level BIST [Benowitz 75]
2. Use only one Signature Register
3. Tests repeat m times to reduce hardware cost

Specific BIST Architecture (2)

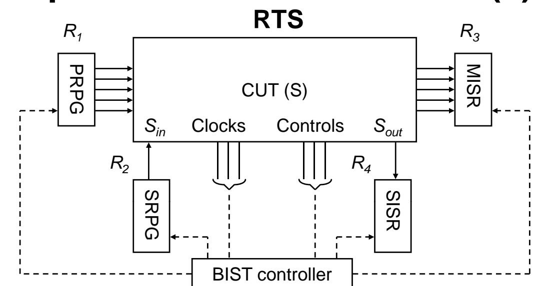


(BEST) (Circular BIST)

1. Pseudo random testing
2. Hardware overhead is low
3. Test length can be long for CUT with random-pattern resistant faults.

Specific BIST Architecture (3)

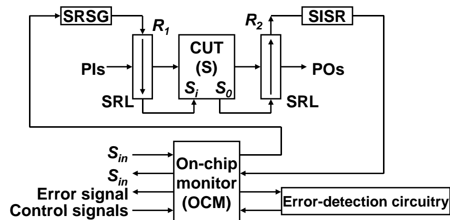
RTS



1. Combine LSSD Scan Chain and BIST
2. Can insert scan points to reduce test length for random-pattern resistant faults

Specific BIST Architecture (4)

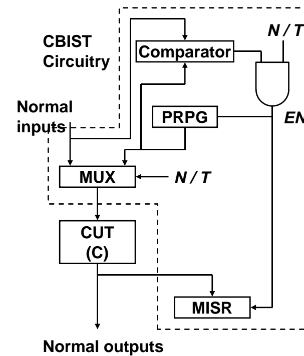
LOCST



1. Boundary scan is required to unify the test architecture
2. Single scan chain may cause high test time overhead.

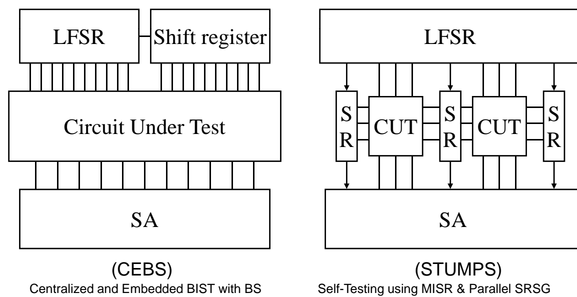
Specific BIST Architecture (5)

CBIST



1. Detect test patterns from normal inputs sequence
2. Once a pattern is detected, compress the response and tick the test clock.
3. If waited too long, insert a test pattern from PRPG.

Specific BIST Architecture (6)



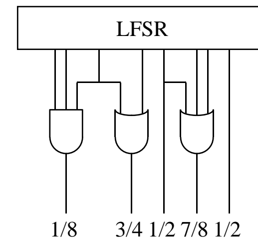
(CEBS)
Centralized and Embedded BIST with BS

(STUMPS)
Self-Testing using MISR & Parallel SRSG

low cost version of RTS or LOCST

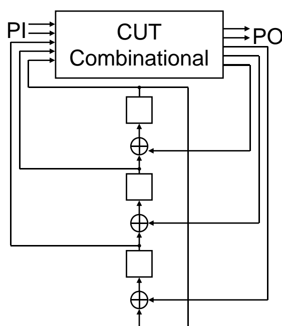
Specific BIST Architecture (7)

LFSR Based
Weighted Pseudo Random Test



Specific BIST Architecture (8)

SST



1. Similar to MISR but without LFSR part

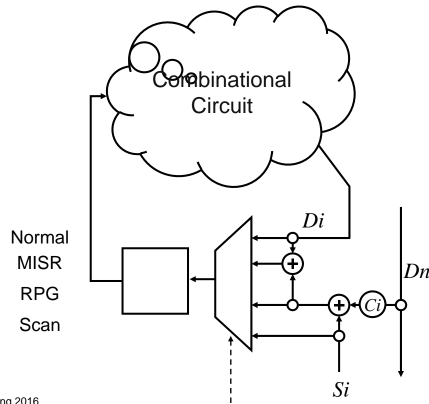
Specific BIST Architecture (9)

HP Focus Chip (Stored Pattern)

1. Chip Summaries
   1. 450,000 NMOS devices, 300,000 Nodes
   2. 24MHz Clocks, 300K bits of on-chip ROM
   3. Used in HP9000-500 computer
2. BIST Micro-program
   1. Use microinstructions dedicated for testing
   2. 100K-bit BIST micro program in CPU ROM
   3. Executes 20 million clock cycles
   4. Greater than 95% stuck-at coverage
   5. A power-up test used in system test, filed test, and wafer test

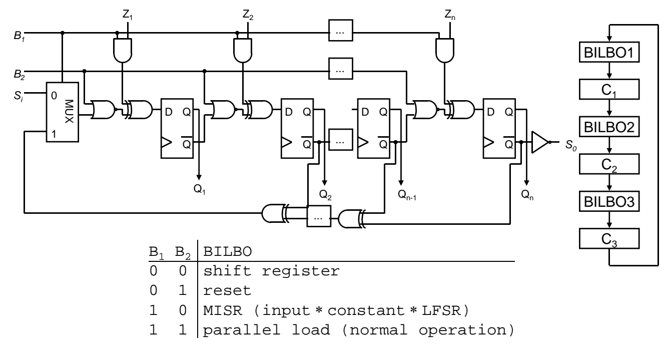
Specific BIST Architecture (10A)

Motivation of BILBO



Specific BIST Architecture (10B)

Built-in Logic Block Observation (Koenemann '79)



B_1	B_2	BILBO
0	0	shift register
0	1	reset
1	0	MISR (input * constant * LFSR)
1	1	parallel load (normal operation)