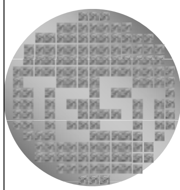

VLSI Test

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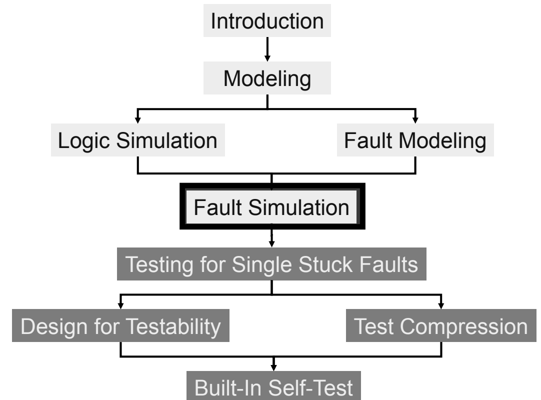
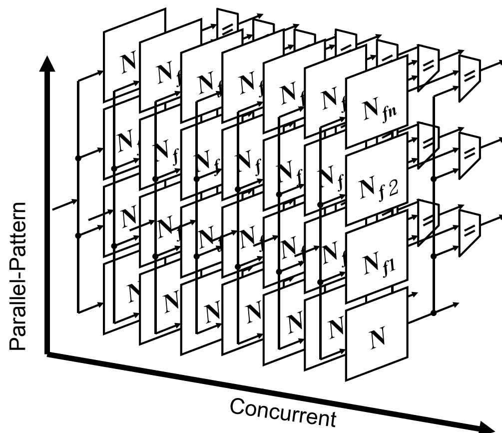
2016/03/07

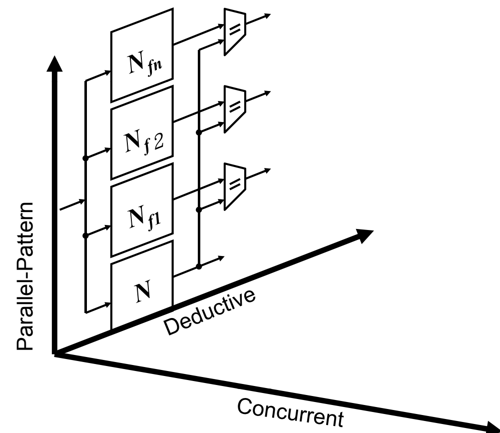
Syllabus & Chapter Precedence



Fault Simulation



Fault Simulation



Applications

1. Evaluate (grade) a test (set) T.
2. Fault Dropping for Test Generation.
3. Construct fault dictionaries before testing for test compaction
4. Construct fault dictionaries for Post-test Diagnosis.
5. Analyze the operation of a circuit in the presence of the faults.

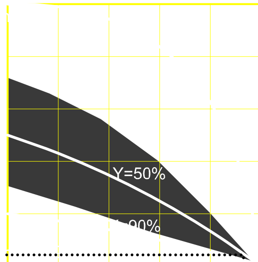
Defect Coverage

- Experience has shown that a test with high Fault Converage (FC) for SSFs also achieve a high DC.
- Defect Level (DL) is defined as the probability of shipping a defective product.

Defect Coverage

Yield (Y) is defined as the probability that a manufactured circuit is defect-free.

- One model gives $DL=1-Y^{1-d}$.



Example

1. Consider all SSFs before collapsing, assume there are 10000 faults and 2000 faults are redundant. Test set T1 can detect 8000 non-redundant faults while T2 can detect only 7200 non-redundant faults. Find their fault coverage (FC) and test efficiency (TE, test coverage for some tools)?

Ans. FC(T1)=8000/10000= 80%
FC(T2)=7200/10000= 72%
TE(T1)= 8000/ 8000=100%
TE(T2)= 7200/ 8000= 90%

Review Fault Collapsing & Dropping

Illustrating by Fault Dictionary

Fault \ Pattern	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}	t_{11}	∞
f_1		1			1			1				
f_2												
f_3			1	1		1				1		
f_4			1	1		1				1		
f_5												?
f_6		1		1	1		1		1		1	
f_7		1		1			1				1	
f_8		1		1			1				1	
f_9	1											

Redundant Fault
← Equivalent Fault
$f_3=f_4$
Abandoned Fault
← Dominant Fault
← Equivalent Fault
$f_6>f_7=f_8$

Review Fault Collapsing & Dropping

Illustrating by Fault Dictionary

↑Fault Collapsing (folding)

Fault \ Pattern	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}	t_{11}	?
f_1		1			1			1				
f_2												
f_3			1	1		1				1		
f_4			1	1		1				1		
f_5												?
f_6		1		1	1		1		1		1	
f_7		1		1			1				1	
f_8		1		1			1				1	
f_9	1											

Review Fault Collapsing & Dropping

Illustrating by Fault Dictionary

Fault Dropping↘

Fault \ Pattern	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}	t_{11}	?
f_1		1			1			1				
f_2												
f_3			1	1		1				1		
f_5												?
f_6		1		1	1		1		1		1	
f_9	1											

Review Fault Collapsing & Dropping

Illustrating by Fault Dictionary

Fault Dropping↘

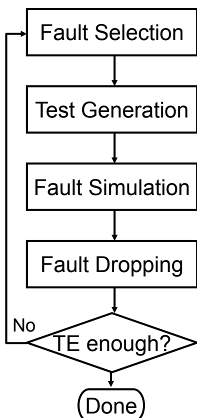
Fault \ Pattern	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}	t_{11}	?
f_1		1			1			1				
f_3			1	1		1				1		
f_6		1		1	1		1		1		1	

Essential Fault

Fault	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}	t_{11}	?
f_9	1											

Fault Grading: $g(f_9)>g(f_1)$ and $g(f_6)>g(f_7)=g(f_8)$ if $f_6>f_7=f_8$

Fault Dropping by Fault Simulation

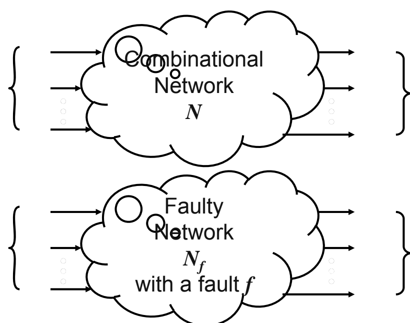


Classification of Fault Simulations

1. Serial
   - Simulate one fault at a time.
2. Parallel
   - Simulate W (>1) faults at a time.
3. Deductive
   - Simulate the good circuit and deduces the behavior of all faulty circuits.
4. Concurrent
   - Simulate only elements that are different from the corresponding ones.

Serial Fault Simulations

1. Simplest and able to handle of any type of faults.



2. (#Faults + 1) times.

Tasks of Fault Simulations

1. Fault Specification
   - Fault modeling and definition
   - Fault collapsing
2. Fault Insertion
   - Fault selection and creation in internal data structure
3. Fault Propagation
   - Occupy most work to propagate the effects.
4. Fault Detection & Discarding
   - Voltage or current signal; analog allowance or digital values.
   - A fault detected for k times should be discarded, usually k=1.

Parallel Simulation

1. Parallel-Fault Fault Simulation: A good circuit and W independent faulty circuits are simultaneously simulated for $\lceil (F+1)/W \rceil$ passes.
2. Parallel-Pattern Simulation: E.g., a 32-bit integer is early used for one bit in serial simulation and 32 bits in PPFP.
3. PPSFP for SSFs.

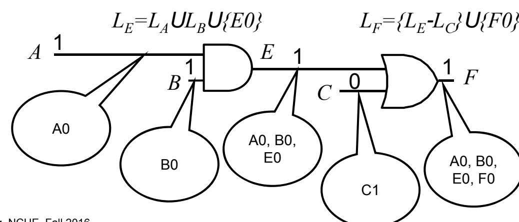
   i =0 or 1

1	1	1	0	1	0	1	1	0	1	1	1	1	1	1	1	0	0	0	1	1	1	1	1	0	1	1	1	0	1	0	1

3. 2 bits required for 3-value or 4-value logic, say {0, 1, u} and {0, 1, D, D'}. (where D=good1/faulty0=↓=s-a-0)
4. Parallel-Pattern Fault Simulation: E.g., a 32-bit integer is early used for one bit in serial simulation and 32 bits in PPFP.

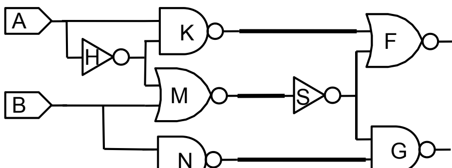
Deductive Fault Simulation

1. Fault List at wire i: the set of all faults that cause the values of I in N and N_f to be different at the current simulated time.
2. Memory for a G-wire circuit with F faults: $G(F+1)$ ~ O(G^2).
3. For a gate Z with controlling value c and inversion i:
4. A simple example of Fault-List Propagation:



Example of TPG-FS-FD (1) SAF List

A0
A1
B0
B1
C0
C1
Ha0
Ha1
H0
H1
Ka0
Ka1
Kb0
Kb1
K0
K1

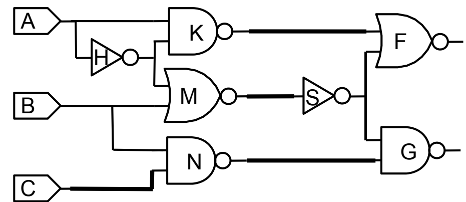


Ma0
Ma1
Mb0
Mb1
M0
M1
Na0
Na1
N0
N1
S0
S1
Fb0
Fb1
F0
F1
Ga0
Ga1
G0
G1

#Single Pin Stuck-At Faults = 44

#Single Line Stuck-At Faults = 44 – 8 = 36

Example of TPG-FS-FD (2) SGSAF List



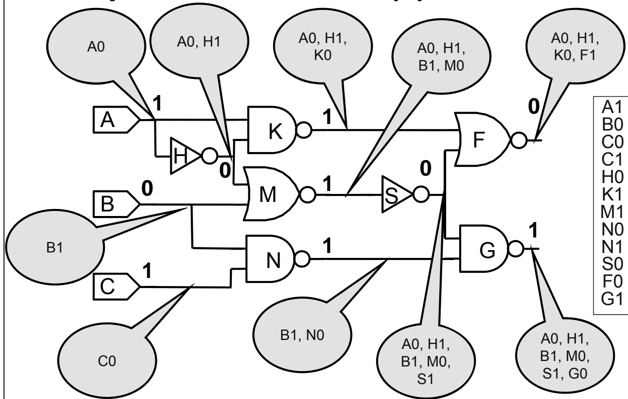
A0
A1
B0
B1
C0
C1
H0
H1
K0
K1
M0
M1
N0
N1
S0
S1
F0
F1
G0
G1

#Single Pin Stuck-At Faults = 44

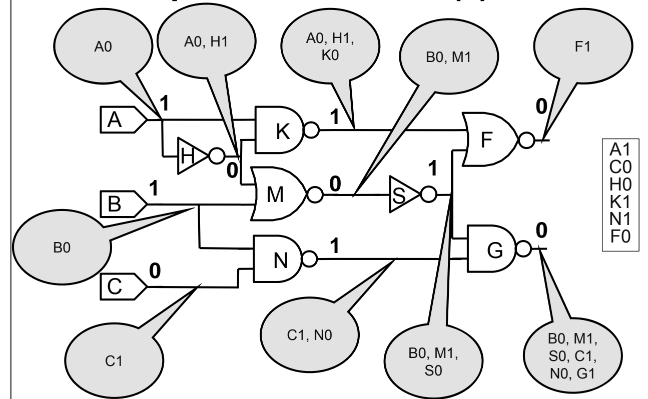
#Single Line Stuck-At Faults = 44 – 8 = 36

#Single Gate Stuck-At Faults = 10 x 2 = 20

Example of TPG-FS-FD (3) Random Test

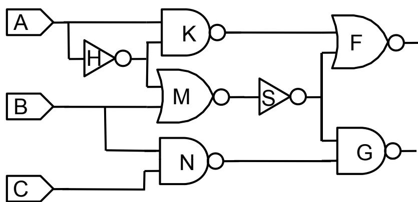


Example of TPG-FS-FD (4) RT-FS



A1
C0
H0
K1
N1
F0

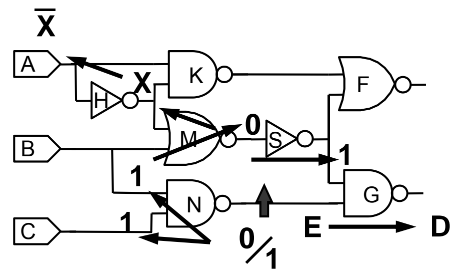
Ex. of TPG-FS-FD (5) Fault Coverage



TS1 = { (ABC, FG) }= { (101,01), (110,00) }

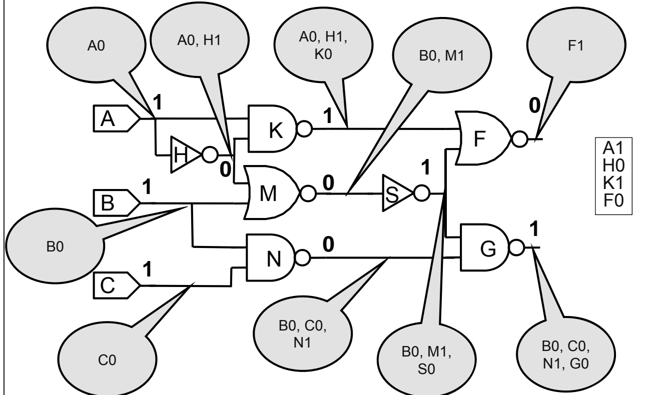
FC(TS1) = 14/20 = 70%

Example of TPG-FS-FD (6) TPG

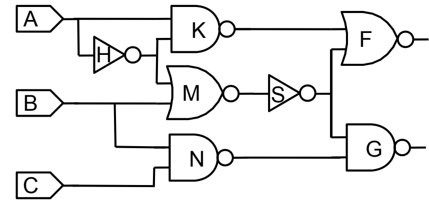


$= \text{ - Difference} = \overline{D} \ (= E)$

Example of TPG-FS-FD (7) TG-FS



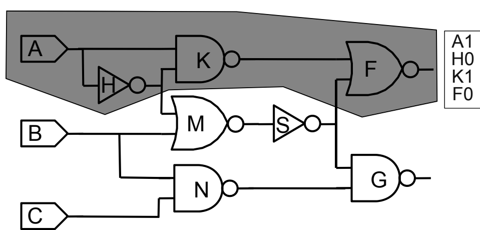
Ex. of TPG-FS-FD (8) Fault Coverage



TS2 = { (ABC, FG) }= { (101,01), (110,00), (111,10) }

FC(TS2) = 16/20 = 80%

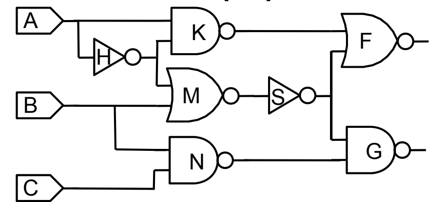
Example of TPG-FS-FD (9) Redundant



Redundant Circuit ➔ Redundant Faults

➔ Undetectable Faults

Ex. of TPG-FS-FD (10) Test Coverage



TS1 = { (ABC, FG) }= { (101,01), (110,00) }

FC(TS1) = 14/20 = 70%

TC(TS1) = 14/16 = 87.5%

TS2 = { (ABC, FG) }= { (101,01), (110,00), (111,10) }

FC(TS2) = 16/20 = 80%

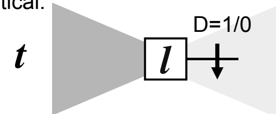
TC(TS2) = 16/16 = 100%

Concurrent Fault Simulation

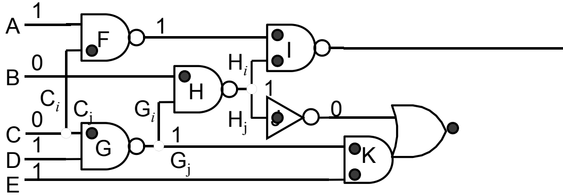
1. Similar to Deductive Fault Simulation but it maintains larger fault list for convenience of executing a Fault-List Event Driven Simulation.
2. A concurrent simulator processes only the active faulty circuits.
3. The main disadvantage of concurrent simulation is that it requires more memory than the other methods.

Critical Path Tracing

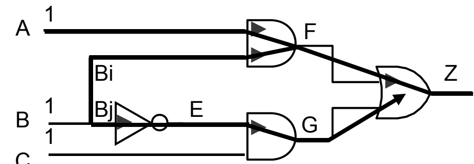
1. A line l has a critical value v in the test (vector) t iff t detects the fault l s-a-$!v$. A line with a critical value in t is said to be critical in t.
2. POs are critical and the others are found by backtracing.
3. Paths composed of critical lines are critical paths.
4. A gate input is sensitive (in a test t) if complementing its value changes the value of the gate output.
5. If a gate output is critical, then its sensitive inputs, if any, are also critical.



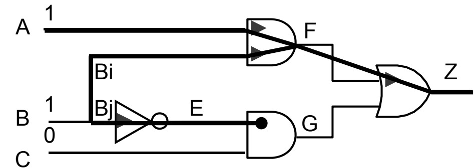
Example



Self-Masking



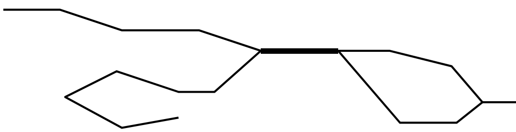
Stem B is self-masking.



Stem B is critial.

Capture Line

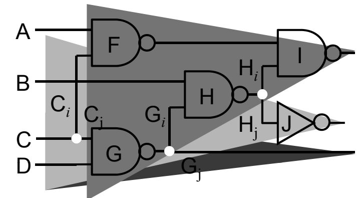
1. Let t be a test that activates fault f in a single-output combinational circuit. Let y be a line with level l_y, sensitized to f by t. If every path sensitized to f either goes through y or does not reach any line with level greater than l_y, then y is said to be a capture line of f in test t.
2. A capture is a bottleneck for the propagation of fault effects.



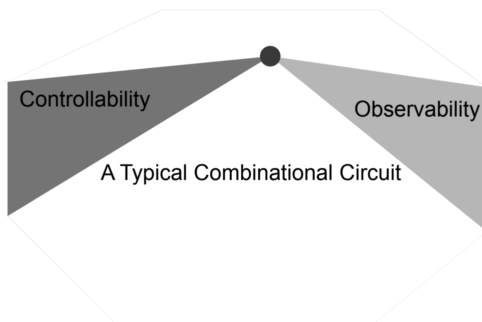
3. A test t detects the fault f iff all the capture lines of f in t are critical in t.

Cones & Fanout-Free Region

1. A Cone contains all the logic feeding one primary output.
2. To take advantage of the simplicity of critical path tracing in fanout-free circuits, within each cone we identify fanout-free regions (FFRs).
3. The inputs of a FFR are checkpoints of the circuit, namely fanout branches and primary inputs. The output of a FFR is either a stem or a primary output.



Testability



STAFAN: Statistical Fault Analysis

Agrawal, 1985

1. Vector-based probability
2. C1(l): The probability causing the output of line l a value v
3. O(l): The probability propagating response from l to any output.
4. Example: