VLSI Test

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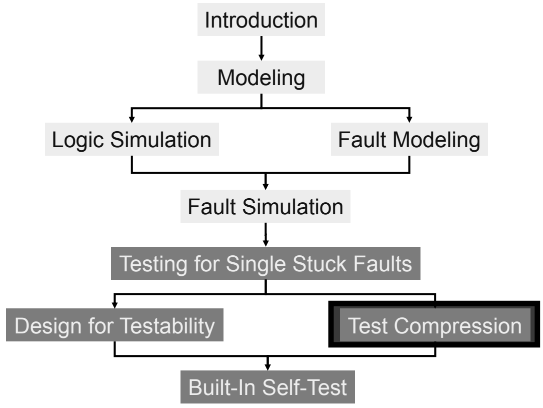
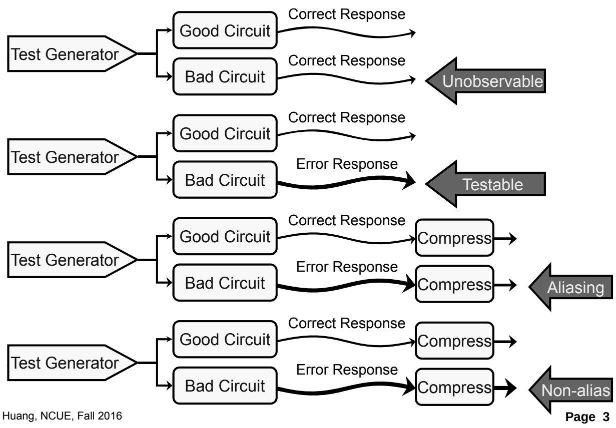
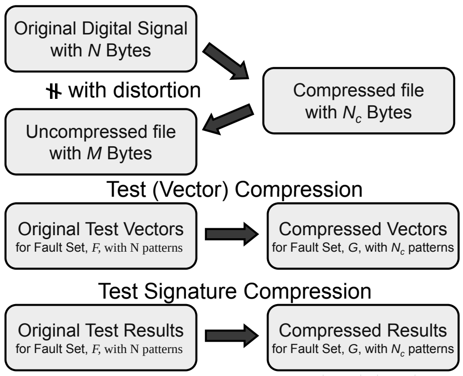
Syllabus & Chapter Precedence



Aliasing



Compression Rate



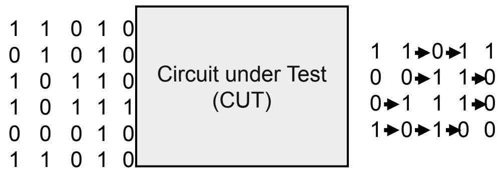
$R = \frac{N - N_c}{N} \times 100\%$

Aliased iff F≠G, alias rate = $a = \frac{|F \setminus G| + |G \setminus F|}{|F|} \times 100\%$

Test Compression Techniques

1. One-Counting
   - #1's in response sequence
2. Transition Counting
   - Transition btw responses r_t and r_{t+1}
3. Parity Checking
   - 0-parity or 1-parity
4. Syndrome Checking
   - ⊂ 1-Counting; 1-ratio in the K-map
5. Signature Analysis
   - Based on CRC (Cyclic Redundancy Check) using LFSR (Linear Feedback Shift Register)

Transition Counting / One-Counting



Compression Rate: $1 - \frac{\log n}{n}$ 1C=11

Aliasing Rate: $Pa = \frac{\binom{n}{r} - 1}{2^n - 1} \cong (\pi n)^{-1/2}$

Compression Rate: $1 - \frac{1}{n}$ Parity Check → Odd

Syndrome Test

- The Syndrome S is the normalized number of ones in the result bit stream based on exhausting test.
- That is, the one-count in the deterministic K-map.
- The syndrome probability can be calculated.

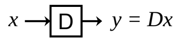
S_1, S_2 → S

AND	S_1S_2
OR	$S_1+S_2-S_1S_2$
NAND	$1-S_1S_2$
NOR	$1-S_1-S_2+S_1S_2$
XOR	$S_1+S_2-2S_1S_2$

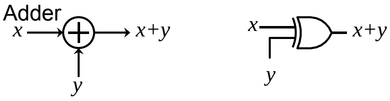
- Not practical in circuitry with many inputs.

Linear Logic Circuit

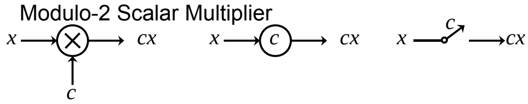
- A linear (logic) circuit preserved the principle of superposition and is constructed from:
  - Delay Flipflops



  - Modulo-2 Adder



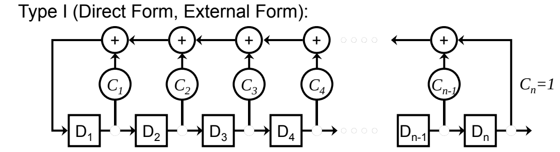
  - Modulo-2 Scalar Multiplier



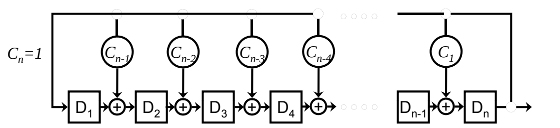
Linear Feedback Shift Register, **LFSR**

- An LFSR can be mapped into a feedback linear circuit with DFFs & XORs in a modulo-2 domain.
- Canonical Forms:

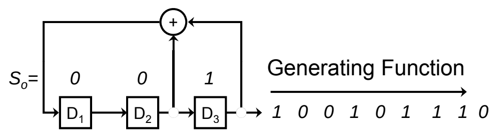
Type I (Direct Form, External Form):



Type II (Indirect Form, Internal Form):



Example



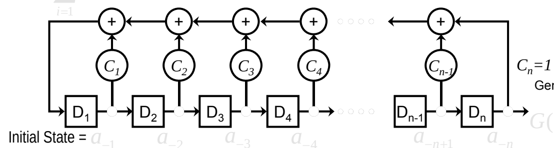
S_1=	1	0	0
S_2=	0	1	0
S_3=	1	0	1
S_4=	1	1	0
S_5=	1	1	1
S_6=	0	1	1
S_7=	0	0	1
S_o=	1	0	0

Why LFSR ?

- Simple and Regular Structure
- Compatible with scan DFT design
- Capable of exhaustive and/or pseudo exhaustive testing
- Low aliasing probability.

Characteristic Polynomials of an LFSR

$$a_m = \sum_{i=1}^{n} c_i a_{m-1}$$



$$G(x) = \sum_{m=0}^{\infty} a_m x^m$$

Initial State = a_{-1} a_{-2} a_{-3} a_{-4} a_{-n+1} a_{-n}

a_{m-1} a_{m-2} a_{m-3} a_{m-4} a_{m-n+1} a_{m-n}

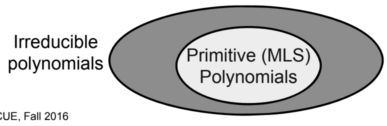
$$G(x) = \sum_{m=0}^{\infty}\sum_{i=1}^{n} c_i a_{m-i} x^m = \sum_{i=1}^{\infty} c_i x^i \sum_{m=0}^{n} a_{m-i} x^{m-i} = \sum_{i=1}^{n} [c_i x^i (\sum_{m=-i}^{-1} a_m x^m + \sum_{m=0}^{\infty} a_m x^m)]$$

$$G(x) = \sum_{i=1}^{n} c_i x^i G(x) + \sum_{i=1}^{n} c_i x^i \sum_{m=-i}^{-1} a_m x^m = \frac{\sum_{i=1}^{n} c_i x^i \sum_{m=-i}^{-1} a_m x^m}{1+\sum_{i=1}^{n} c_i x^i} = \frac{1}{P(x)}$$ If IS=1 at D_n.

Characteristic polynomial $P(x)$

Maximum Length Sequence

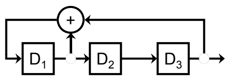
- Let p be the generating period, $P(x)$ divides into $1-x^p$.
- Reciprocal polynomial of P(x) is $P^*(x)=x^nP(1/x)$.
- If $G(x)$ of an n-stage LFSR has period 2^{n-1}, then it is called a maximum-length sequence (MLS) and the characteristic polynomial is called a primitive polynomial.
- An irreducible polynomial $P(x)$ is with odd number of terms and it's primitive if $min(k)=n$ for .



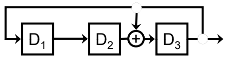
An Algorithm to Search ML-LFSR

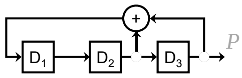
1. *For i=1, x+1 is a primitive polynomial;*
2. *Put searched irreducible polynomials into a queue.*
3. *Check a polynomial of order n with the irreducible polynomial of order less than square-root of n.*
4. *If it is irreducible, check if k is the smallest integer such that it divides into $1+x^k$, where $k=2^{n-1}$.*

Examples of Primitive Polynomials

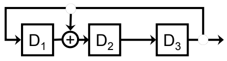


$P(x)=x^3+x+1$
primitive





$P^*(x)=x^3+x^2+1$



x^5+x^2+1

$x^8+x^6+x^5+x+1$

$x^{16}+x^5+x^3+x^2+1$

$x^{32}+x^{28}+x^{27}+x+1$

$x^{36}+x^{11}+1$

Note that $P^*(x)$ must not be primitive even if $P(x)$ primitive.

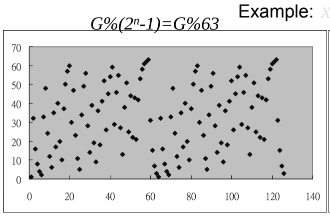
Characteristics of MLS

1. The number of ones in an L-Sequence differs from the number of zeros by 1.
2. An L-Sequence produces an equal number of runs of 1s and 0s.
3. In every L-Sequence, one half the runs have length 1, one fourth have length 2, one eighth have length 3, and so forth.
4. The above properties of randomness make feasible the use of LFSRs as test sequence generators in BIST (Built-In Self-Test, introduced in next chapter) circuitry.
5. LFSRs used as counters are taken advantage of its speed (usually with only the exclusive gate for propagation time of the combinational circuits)

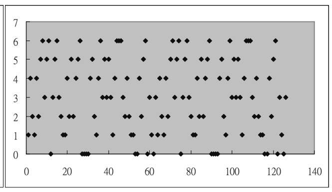
Pseudo Randomness

Example: x^6+x^5+1

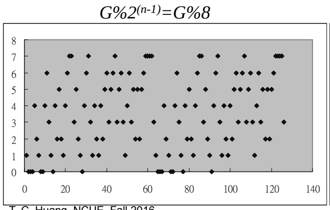
G%(2^n-1)=G%63



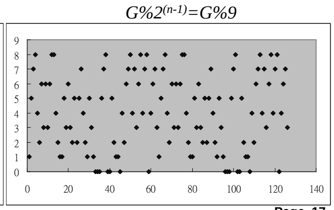
G%2^(n-1)=G%7



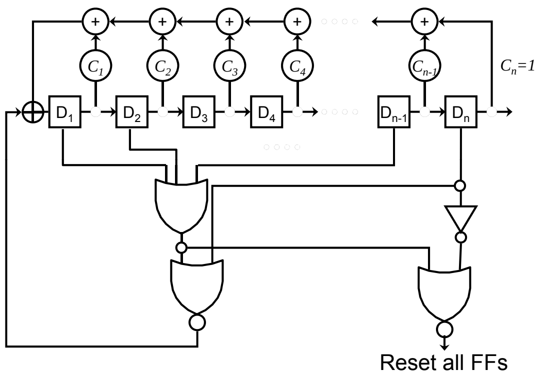
G%2^(n-1)=G%8



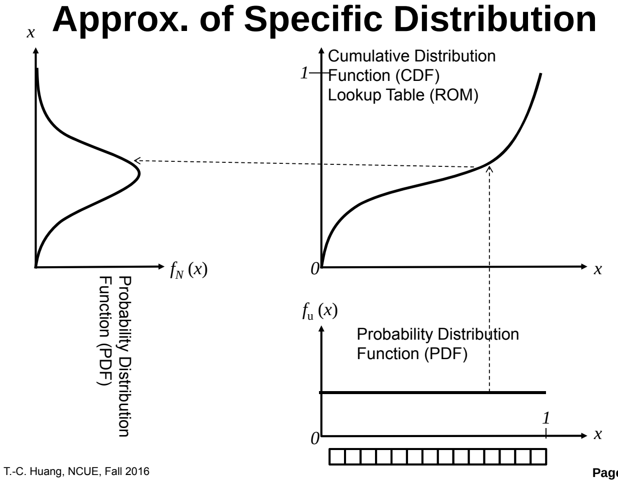
G%2^(n-1)=G%9



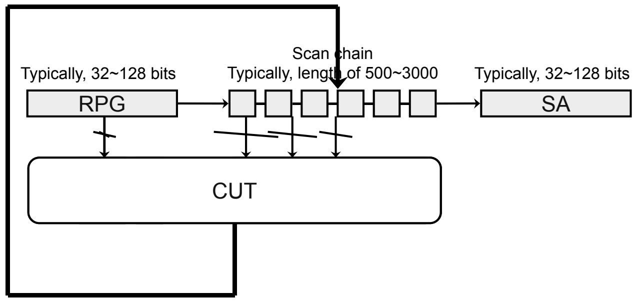
LFSR with the All-Zero Pattern



Approx. of Specific Distribution

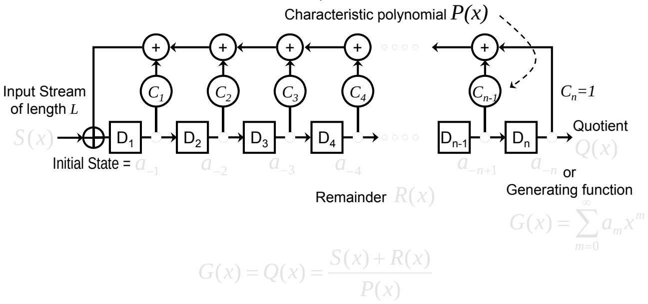


(Pseudo) Random Pattern Generator **(RPG)**



Signature Analyzer (SA)

- Signature Analysis is a compression technique based on the concept of cyclic redundancy checking (CRC).
- We use S(x) to denote the input stream (instead of G(x) that is confused in textbook).



Signature Analyzer (SA)

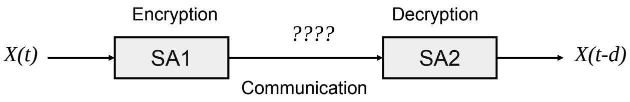
RPG as a special case of SA: $S(x)=0$ and $R(x)=\sum_{i=1}^{n} c_i x^i \sum_{m=-i}^{-1} a_m x^m$

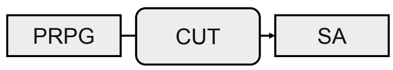
There are 2^L possible input stream, 2^{L-n} streams produce a signature.

Aliasing rate (proportion of masking error streams is $\frac{2^{L-n}-1}{2^L-1} \approx 2^{-n}$

SA with >1 non-0 coefficients detects all single-bit errors (e.g. $x+1$).

Two Different Application Examples

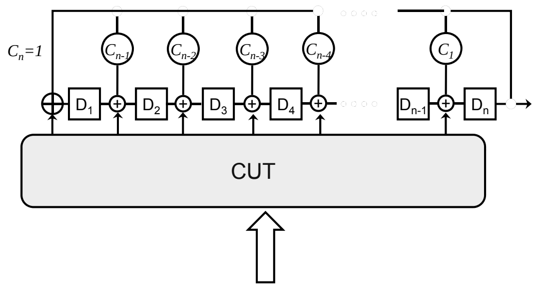




Testing

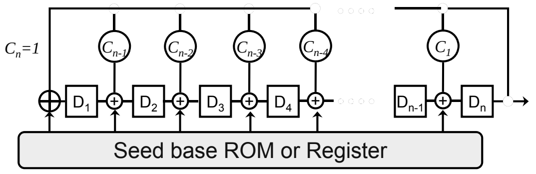
Multiple Input Signature Register **(MISR)**

Only Type II (Internal) forms can be improved to be multiple-input.



Can be RPG or Non-Random Patterns (e.g., Counter)

Multiple Inputs Used in Seed Loading



Integrated RPG/MISR into Scan Cells