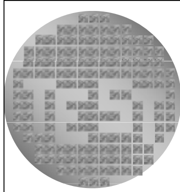

VLSI Test

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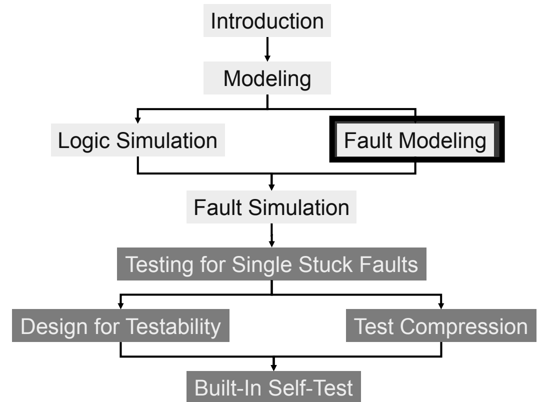
Syllabus & Chapter Precedence



Related to Faults

1. **System Failure: System doesn't work.**
2. **Error: Incorrect operation of a system, that possibly works.**
   - Design errors
   - Physical Faults
3. **Physical Fault: incorrect operation of a modeled element due to Fab.**
   - Fabrication errors
     - Wrong components
     - Incorrect wiring or shorts
   - Physical Defects

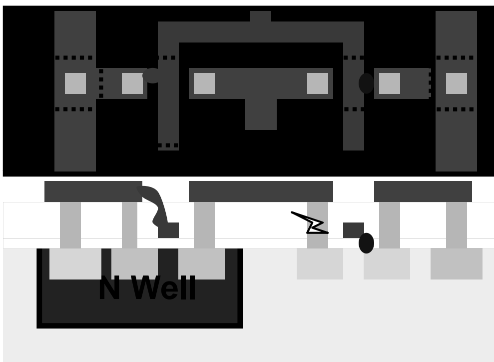
   Classified according to time stability:
   - Permanent
   - Intermittent
   - Transient
4. **Physical Defect:**
   - Fabrication defects
   - Physical failure

Physical Faults

1. **Logical Faults: the effect of physical fault on the behavior of the modeled system.**
   - Faults that affect the objective function
   - Delay faults
2. **Modeling physical faults to logical faults:**
   - Complexity reduction
   - Technology-independent
   - Tests may be used even if behavior unknown
3. **Views:**
   - Structural faults
     - (Wire, transistor) Short/open
     - Stuck-at
     - Bridging fault
   - Functional faults
4. **Simultaneous occurrence:**
   - Single-fault assumption
   - Multiple-fault

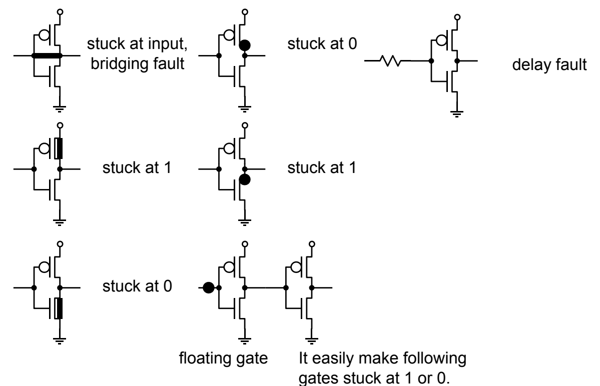
Inductive Fault Analysis

Investigate what and how more physical faults induce to high-level faults.

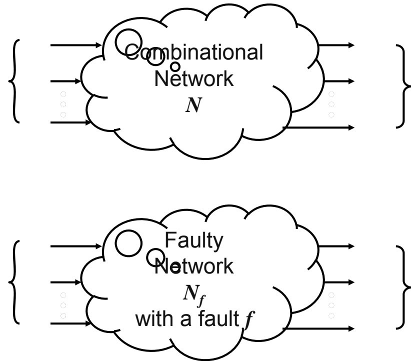


Inductive Fault Analysis

Examples

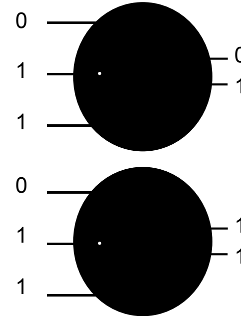


Fault Detection of Combinational Circuits



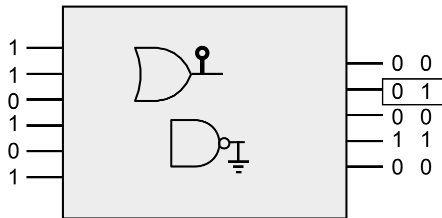
Test Vector

1. **A test (vector) t detects a fault $f \Leftrightarrow Z_f(t) \neq Z(t)$.**
2. **Example: a fault with a component error**



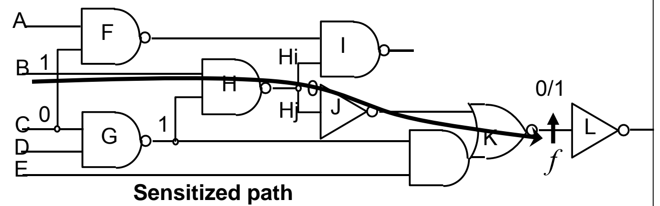
Test Vector

1. **A test (vector) t detects a fault $f \Leftrightarrow Z_f(t) \neq Z(t)$.**
2. **Example: Multiple Stuck-At Faults**



Sensitization

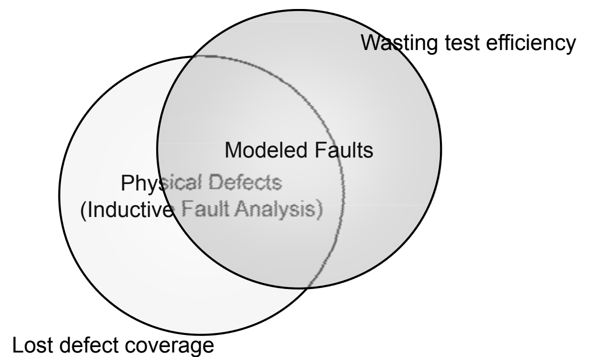
1. A line whose value in the test t changes in the presence of the fault f is said to be sensitized to the fault f by the test t.
2. Example: C17 in ISCAS85 benchmark



Fault Models

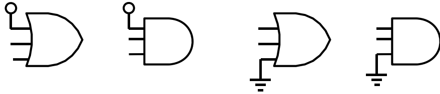
1. For Logic Circuits:
   1. Transistor Level:
      - Stuck-Open Fault
      - Bridging Fault
      - Transistor Stuck On/Off Fault
   2. Gate Level:
      - Gate-Output Bridging Fault
      - Delay Fault: {path, segment, gate} delay fault
        Why not cone delay fault?
      - Gate-Output Stuck-At Fault
        - Single Stuck-At (SSA) Fault
        - Multiple Stuck-At (MSA) Fault
2. For Memory:
   - SSA, MSA, Coupling Fault, Transition Fault, …
3. State Machine:
   - State Transition Fault, …

Correctness of a Fault Model

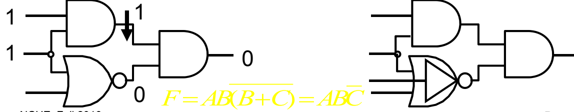


Detectability & Redundancy

1. A fault f is said to be detectable if there exists a test t that detect f; otherwise, undetectable.
2. A combinational circuit that contains an undetectable stuck fault is said to be redundant, since such a circuit can always be simplified by removing at least one gate or gate input.
3. Trivially (directly) redundant gate (input):

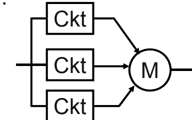


4. Undetectable → Somewhere redundant → Reducable



Detectability & Redundancy

4. Some meaningful redundant circuits:
   1. TMR (Triple modular redundancy) for fault-tolerant design.



   2. Hazard masking gate

AB \ C	0	1
00	0	0
01	0	1
11	1	1
10	1	0

$F = \overline{A}C + BC + AB$

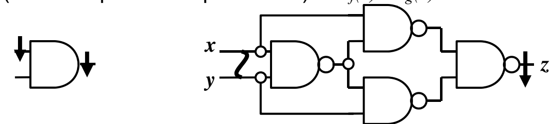
   3. Dummy circuits for matching or cancellation.

Practically Undetectable

1. Redundancy identifying ~ test generation : NP-complete!
2. NP-complete: a problem is said to be NP-complete if no polynomial-time algorithm exists.
   (Usually it can be solved in polynomial-time for most instances, but at least one instance needs exponential time.)
3. In a practical sense, there is no difference btw an undetectable fault and a detectable one that is not detected by an applied test set.
4. To have a fair test efficiency for a test tool, the definition of the redundant faults (circuits) should be cared.
5. Usually,
   - Fault Coverage = Detected/(Detectable + Undetectable)
   - Test Efficiency = Detected/Detectable

Fault Equivalence

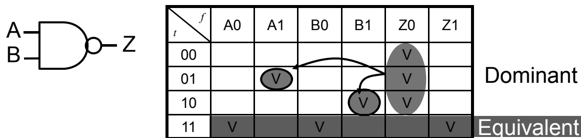
1. Two faults f and g are said to be functionally equivalent (under all possible inputs x E X) ⇔ $Z_f(x)=Z_g(x)$.



2. For any t, $Z_f(t) \neq Z_g(t)$ ⇨ f and g are distinguishable.
3. For fault analysis it is sufficient to consider only one reprehensive fault from every equivalency class.
4. For a gate with controlling value c and inversion i, all the input s-a-c faults and the output s-a-$(c$^$i)$ are functionally equivalent.
5. Equivalence Fault collapsing: Reduction of faults required to analyze based on equivalence.

Fault Dominance

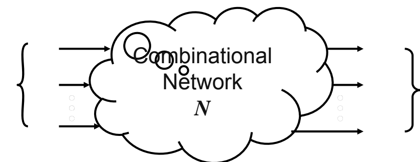
1. Let Tg be the set of all tests that detect a fault g.
2. F dominates g ⇔ $Z_f(Tg)=Z_g(Tg)$.

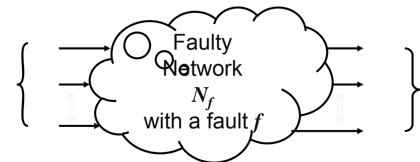


t \ f	A0	A1	B0	B1	Z0	Z1
00					V	
01		V			V	
10				V	V	
11	V		V			V

2. For a gate with controlling value c and inversion i, the output s-a-$(!c$^$i)$ dominates any input s-a-$!c$.
3. Dominance Fault collapsing: Reduction of faults required to analyze based on dominance.

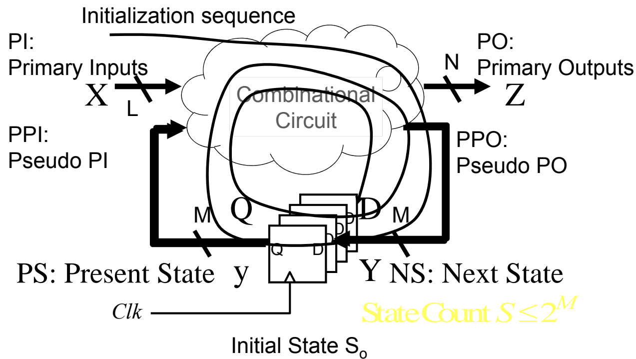
Fault Detection of Sequential Circuits





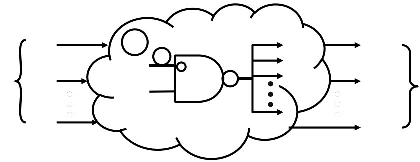
Fault Detection of Sequential Circuits

Single Clock, Synchronous, DFF-based



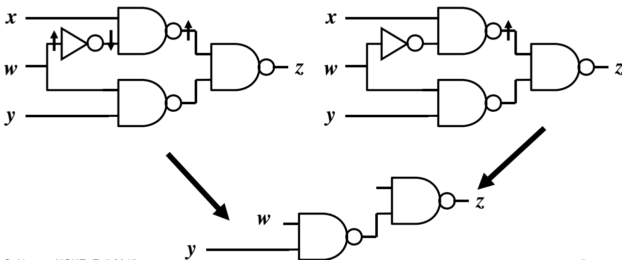
Single Stuck-Fault Model

1. Single Stuck Fault (SSF) model is also referred to as the classical or standard fault model.
2. Most physical defects can be mapped into SSFs.
3. Still popularly used in industry.
4. The fault universe of a circuits with G gates is about $2Gf$, where f is the average fanout count.



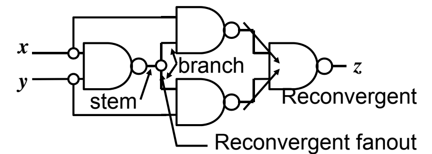
Local Structure Analysis

1. Simplified faulty circuit of circuit N with fault f, $S(N_f)$, is defined as the remaining circuit by removing the stuck lines with a constant values.
2. f and g are structural equivalent ⇔$S(N_f)$=$S(N_g)$⇨Functional eq.
3. Structural equivalence analysis can be done locally while global analysis required for functional equivalence.

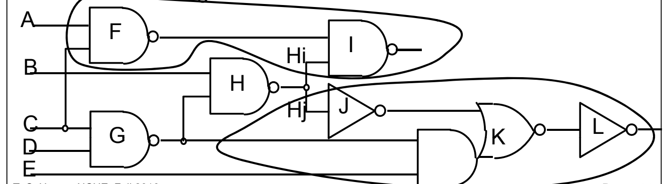


Local Structure Analysis

1. When fanout n of a gate is more than 1, the output wire is called a stem with n branches.

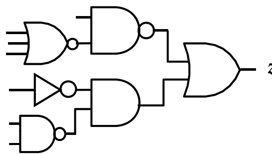


2. Fanout-free region



Fanout-free Combinational Circuits

1. In a fanout-free combinational circuit C, any test set that detects all SSFs on the PIs of C detects all SSFs in C.

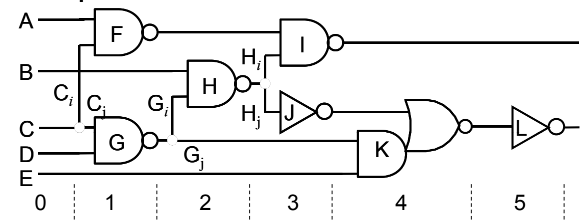


2. In a combinational circuit C, any test set that detect all SSFs on the PIs & the fanout branches of C detects all SSFs in C. The Primary Inputs (PIs) and the Fanout Branches (FBs) are called checkpoints (CPs).
3. The dominance fault collapsing reduces the number of faults dealt with from $2w$ to $2(I+\Sigma b_i)$ (where w, I, b_i are counts of wires, PIs and branches of the ith fanout).

Example

1. C17 in ISCAS85 benchmark:

Checkpoints:



Levelization

w=18, I=5, b_1=2, b_2=2, b_3=2