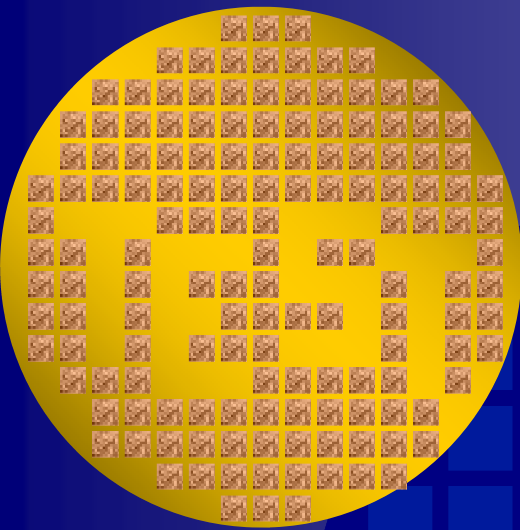

VLSI Testing

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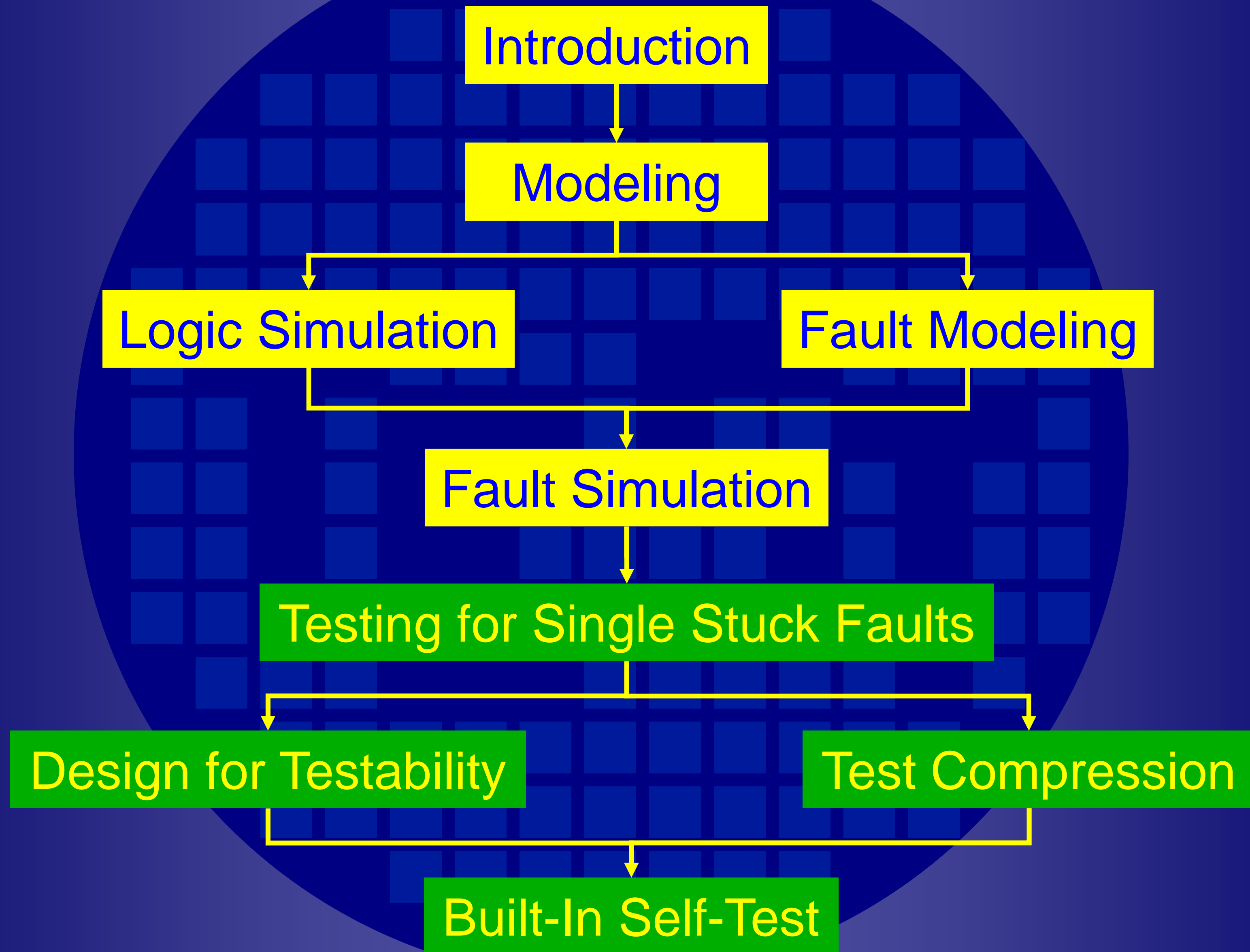
Syllabus & Chapter Precedence



Introduction to IC Test

Outline

1. What's Testing
2. Why Test?
3. Difficulties of Testing
4. How to Do Testing?
5. Logic/Fault Simulations
6. Test Generation
7. Built-In Self-Test
8. Test Compression
9. DFT

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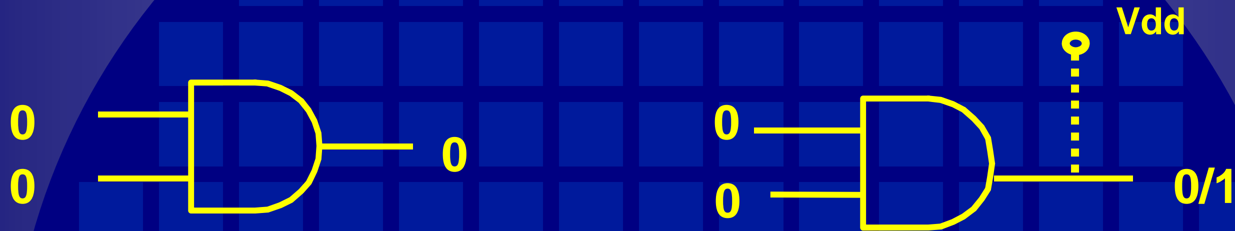
What's Testing

To tell whether a system is good or bad



Related fields

Verification: To verify the correctness of a design

Diagnosis: To tell the faulty site

Fault-tolerance: To work normally even faults exist

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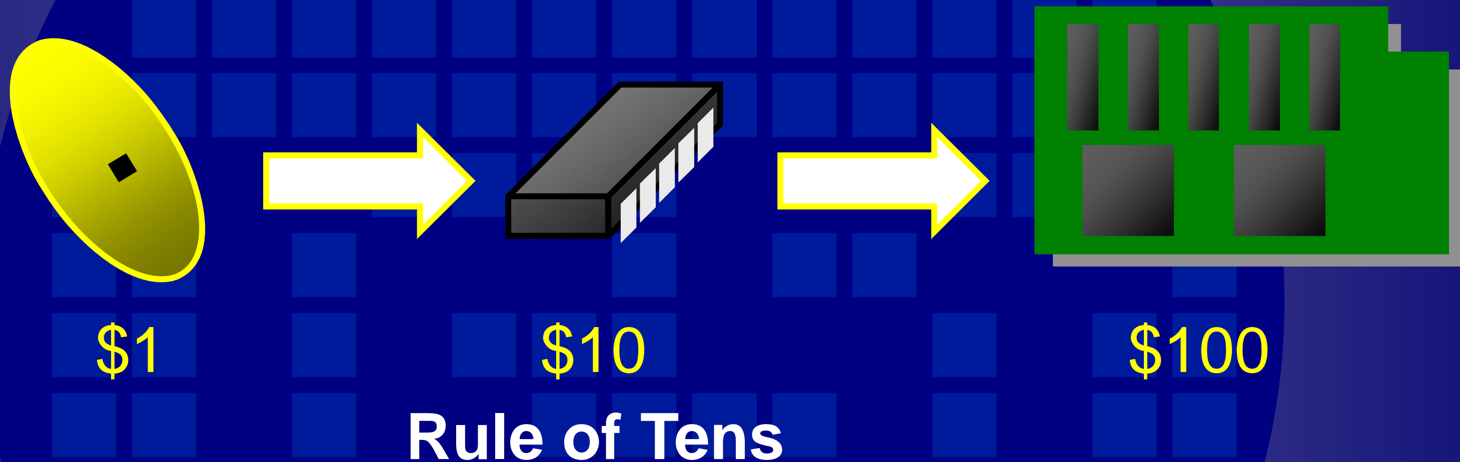
Why Test?

1. Why not ship without test?
2. Why not final product test only?



Rule of Tens

3. Why not functional test only?

- Without test at stage k
- Cost wasted: $(1-Y)(P_{k+1}-P_k)$

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Example for Yield Loss due to Size

Importance of Test

N = # transistors in a chip

p = prob. (a transistor is faulty)

Pf = prob. (the chip is faulty)

→ $Pf = 1 - (1 - p)^N$

If $p = 10^{-6}$

$N = 10^6$

→ Pf = 63.2%

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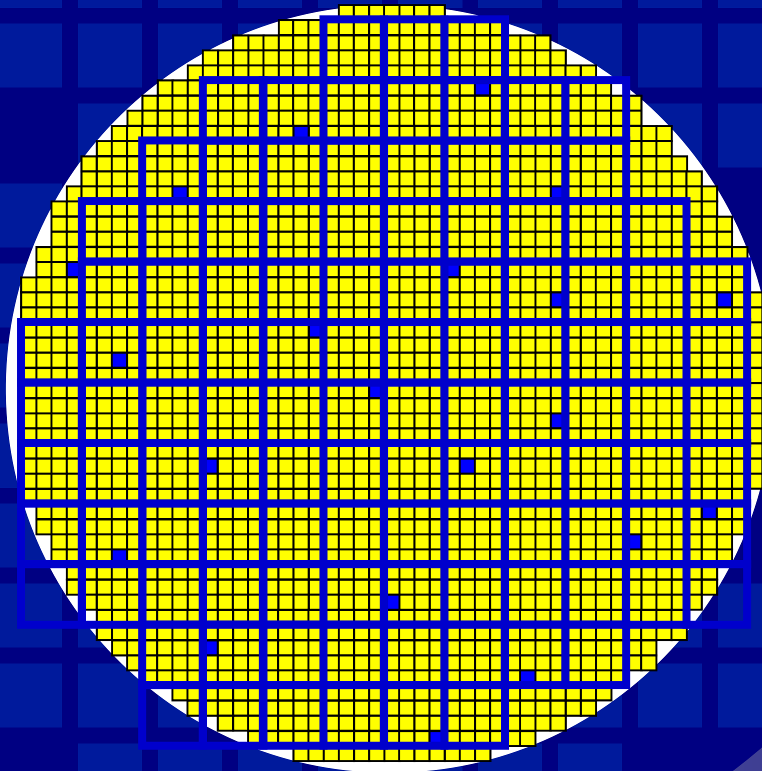
Example for Yield Loss due to Density or Size

When chips are very small, assume the probability of defected chip is α □ Y=1- α



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Why Not Final Product Test Only?

Importance of Test

1. Testability degradation
2. Faults may occur at any phase
3. Average Penalty Increasing

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Why not functional test only?

Problems to think

1. A 32 bit adder
2. A 32 bit count-up counter with RESET function
3. A 1MB cache memory
4. A 10M-transistor CPU

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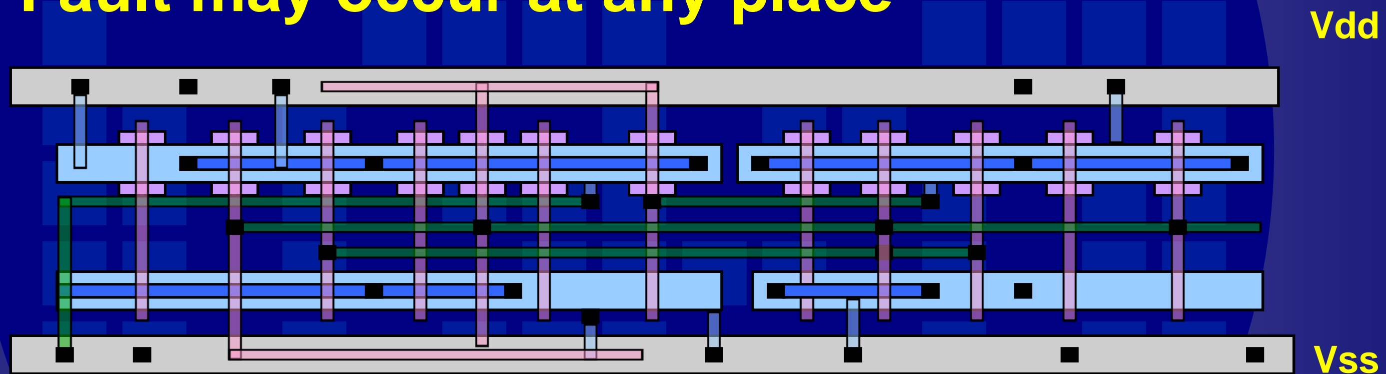
Difficulties in Testing

- **Fault may occur anytime**
  - Design
  - Process
  - Package
  - Field
- **Fault may occur at any place**



- **VLSI circuit are large**
  - Most problems encountered in testing are NP-complete
- **I/O access is limited**

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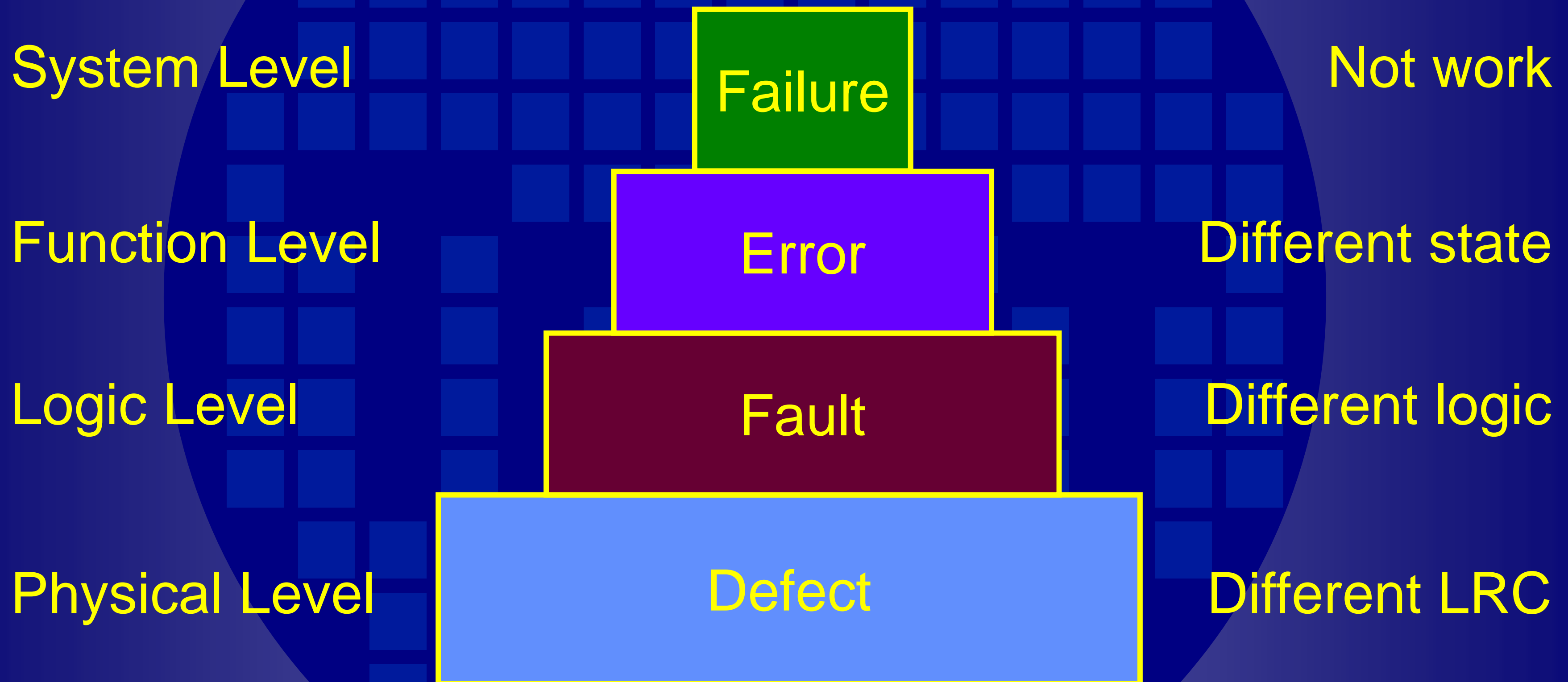
From Defect to Failure



Fault Manifestation

- **Permanent Faults**
- **Non-permanent Faults**
  - ✓ Transient Faults
    - Soft Faults
  - ✓ Intermittent Faults

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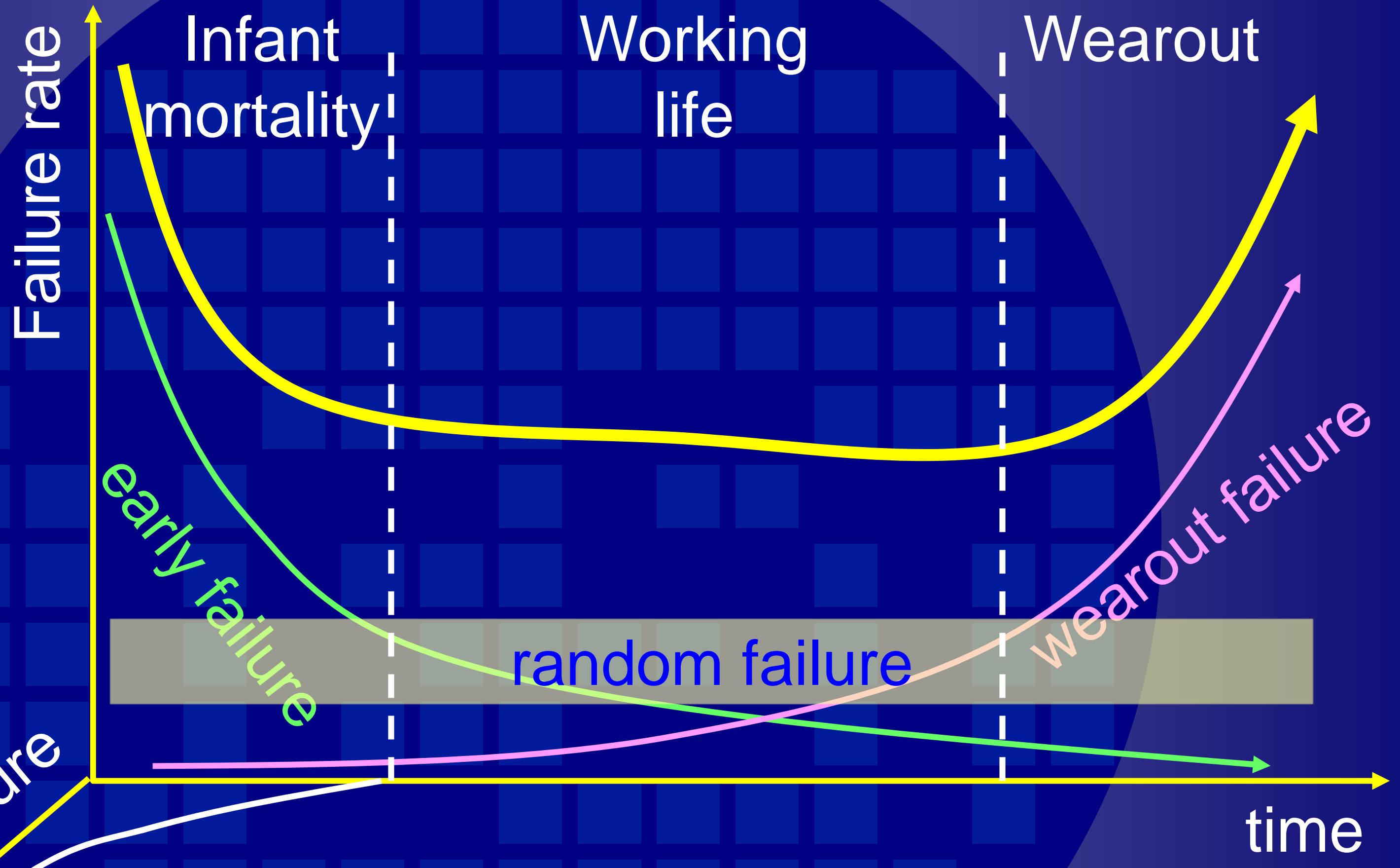
Bathtub Curve



How to Do Testing

- Circuit modeling
- Fault modeling

} Modeling

- Logic simulation
- Fault simulation
- Test generation

} ATPG

- Design for test
- Built-in self test

} Testable design

- Synthesis for testability

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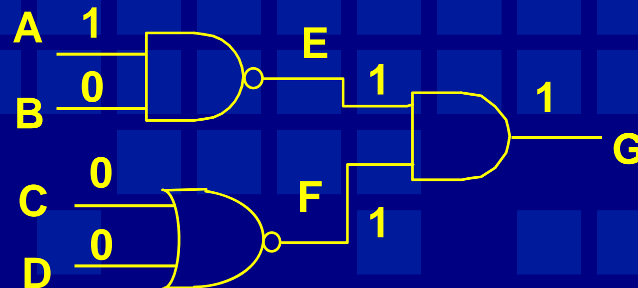
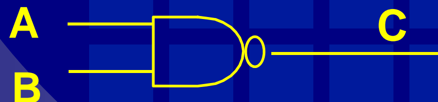
Fault Simulation

- To determine the behavior of faulty circuits



- Given a test vector, determine all faults that are detected by this test vector.

Example:



Test vector (1 1) detects
{ a_0, b_0, c_1}

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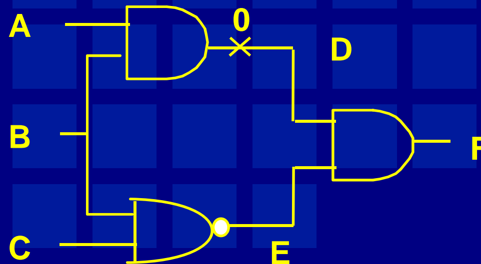
Test Generation

- Given a fault, identify a test to detect this fault

Example:



To detect D s-a-0, D must be set to 1. Thus A=B=1.

To propagate fault effect to the primary output E must be 1. Thus C must be 0.

Test vector: A=1, B=1, C=0

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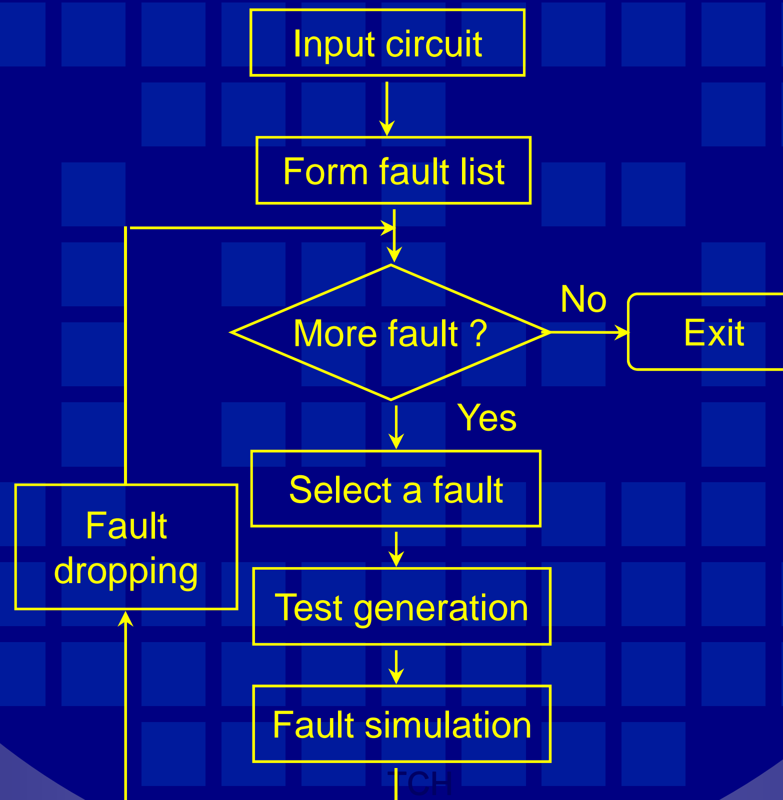
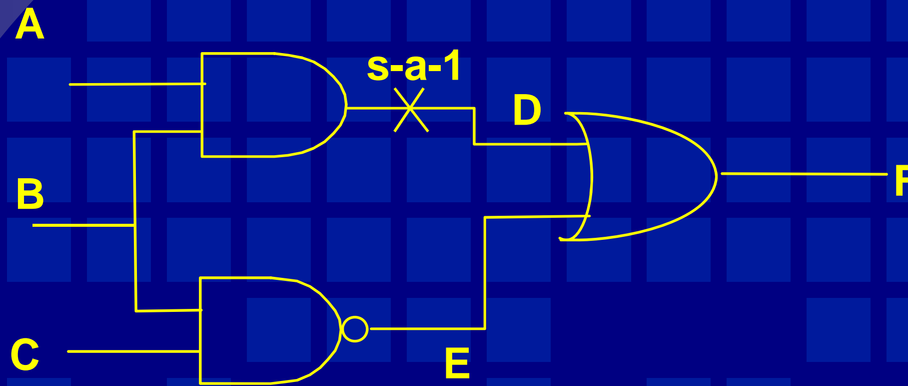
Automatic Test Pattern Generation

- **Given a circuit, identify a set of test vectors to detect all faults under consideration.**

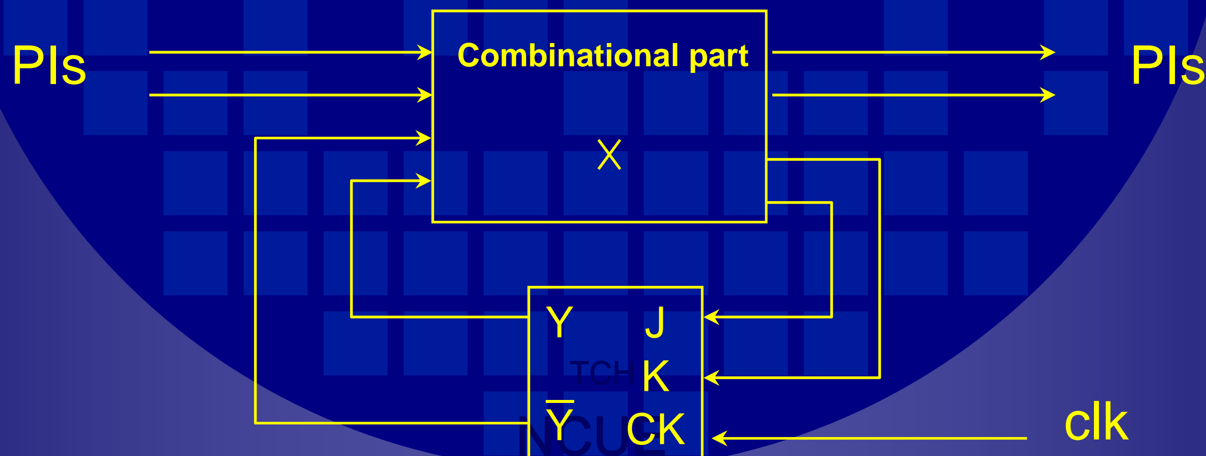


Difficulties in test generation

1. Reconvergent fanout



2. Sequential test generation

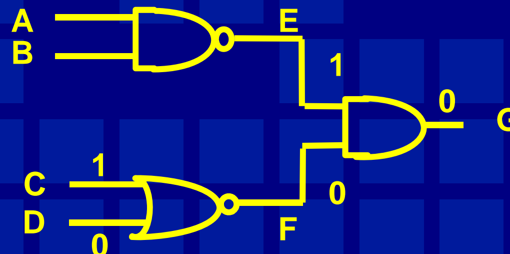


Circuit Modeling

- **Functional model---** logic function
  - **f(x1,x2,...)=...**
  - **Truth table**

- **Behavioral model---** functional + timing
  - **f(x1,x2,...)=... , Delay = 10**

- **Structural model---** collection of interconnected components or elements



⇒ **All can be described in Verilog**

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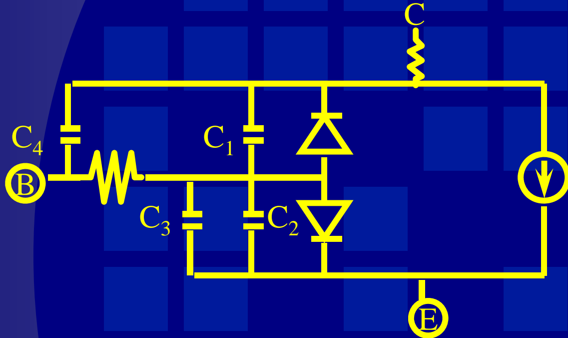
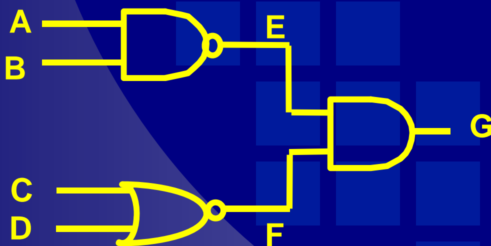
Levels of description

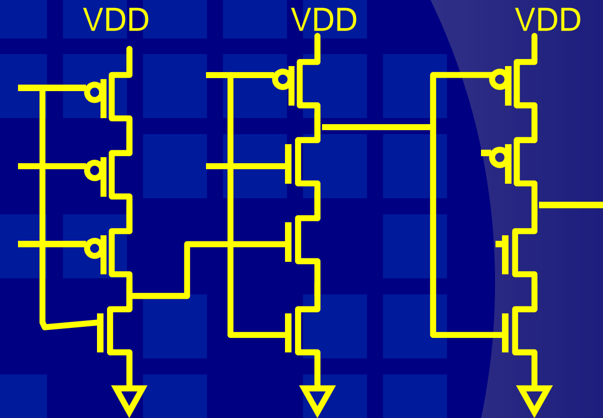
- Circuit level



- Gate level



- Switch level



- Higher/ System level

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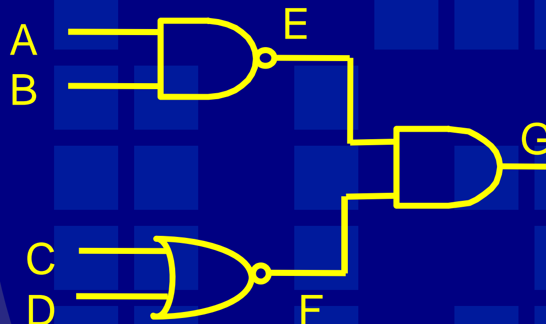
Fault modeling

- **The effects of physical defects**
- **Most commonly used fault model: Single stuck-at fault**



A s-a-1	B s-a-1	C s-a-1	D s-a-1
A s-a-0	B s-a-0	C s-a-0	D s-a-0
E s-a-1	F s-a-1	G s-a-1	
E s-a-0	F s-a-0	G s-a-0	

14 faults

- **Other fault models:**
  - Break faults, Bridging faults, Transistor stuck-open faults , Transistor stuck-on faults, Delay faults

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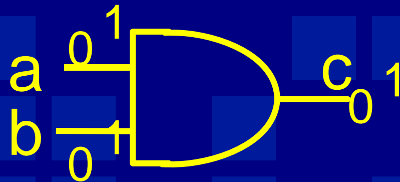
Fault coverage (FC)

$$FC = \frac{\text{\# faults detected}}{\text{\# faults in fault list}}$$

Example:



6 stuck-at faults
($a_0, a_1, b_0, b_1, c_0, c_1$)

Test	faults detected	FC
{(0,0)}	c_1	16.67%
{(0,1)}	a_1, c_1	33.33%
{(1,1)}	a_0, b_0, c_0	50.00%
{(0,0),(1,1)}	a_0, b_0, c_0, c_1	66.67%
{(1,0),(0,1),(1,1)}	all	100.00%

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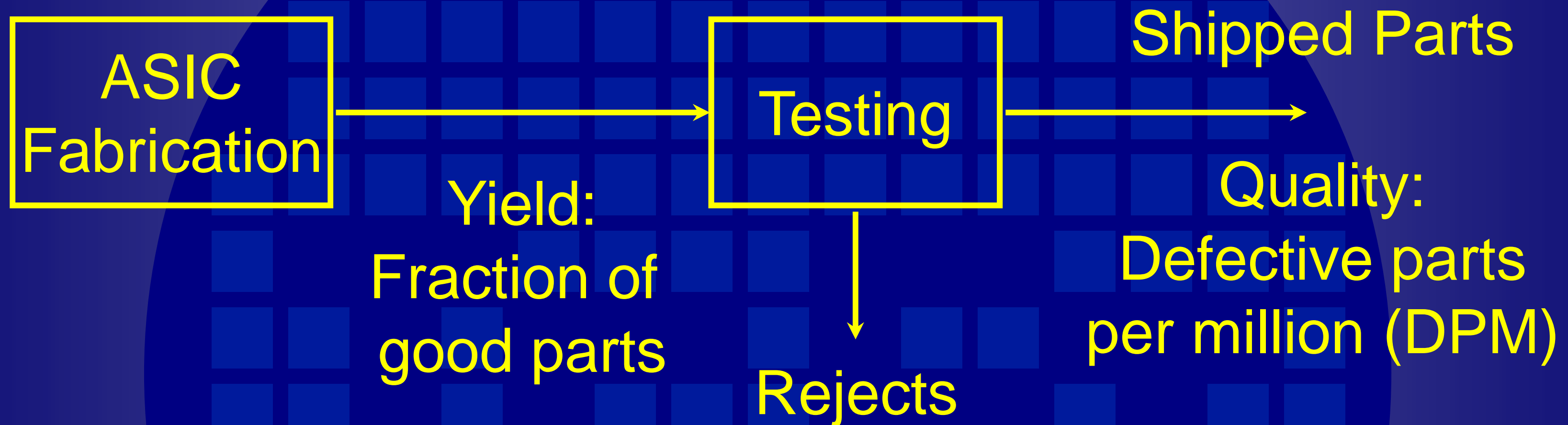
Testing and Quality



- **Quality of shipped parts is a function of yield Y and the test (fault) coverage T**
- **Defect level (DL) : fraction of shipped parts that are defective**

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Defect Level, Yield & Fault Coverage

$$DL = 1 - Y^{(1-T)}$$

DL: defect level

Y: yield

T: fault coverage

Yield (Y)	Fault Coverage (T)	DPM (DL)
50%	90%	67,000
75%	90%	28,000
90%	90%	10,000
95%	90%	5,000
99%	90%	1,000
90%	90%	10,000
90%	95%	5,000
90%	99%	1,000
90%	99.9%	100

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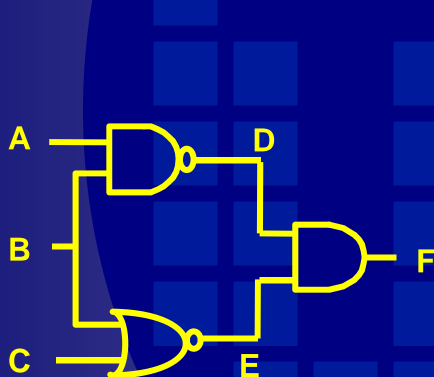
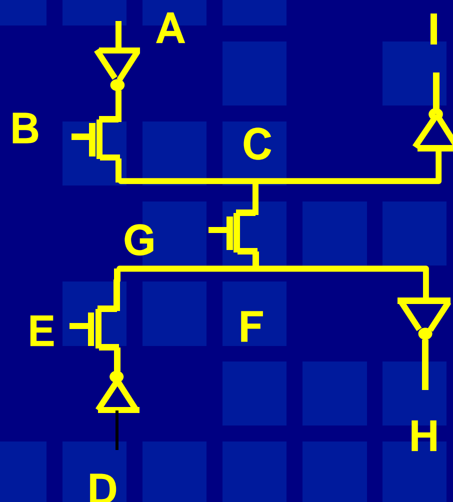
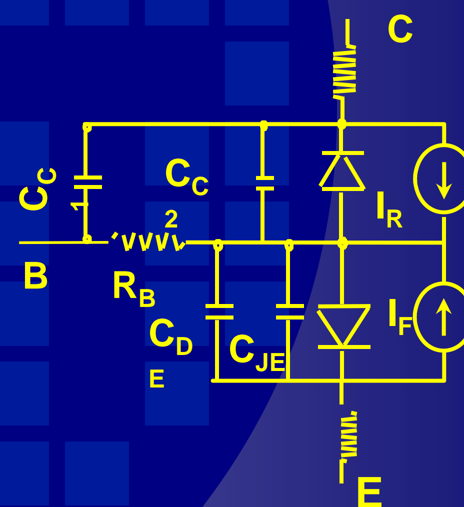
Logic simulation

To determine how a good circuit should work

- Given input vectors, determine the normal circuit response







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Testable Design

- Design for testability (DFT)
  - *ad hoc* techniques
  - Scan design
  - Boundary Scan
- Built-In Self Test (BIST)
  - Random number generator (RNG)
  - Signature Analyzer (SA)
- Synthesis for Testability

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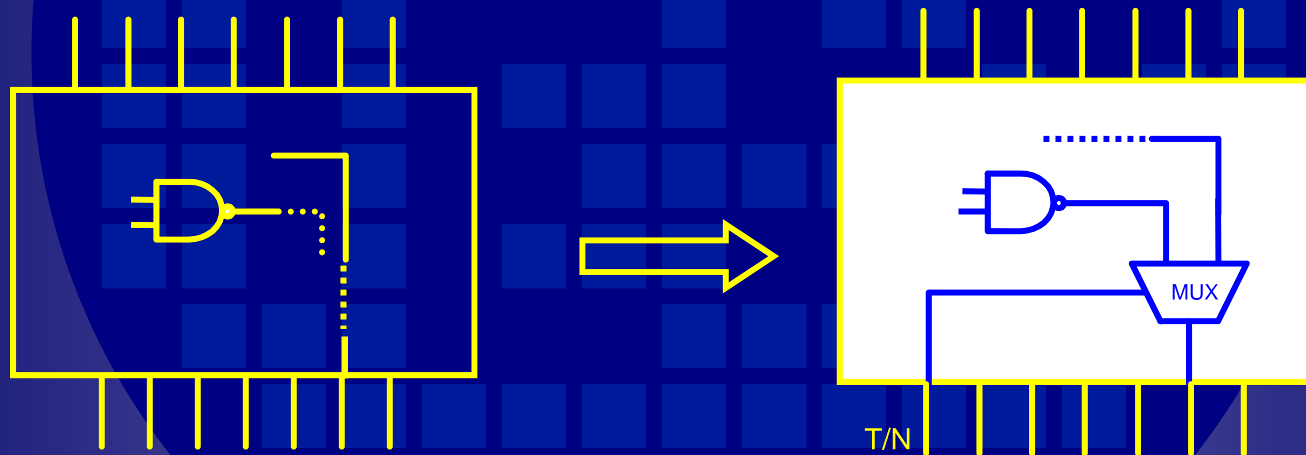
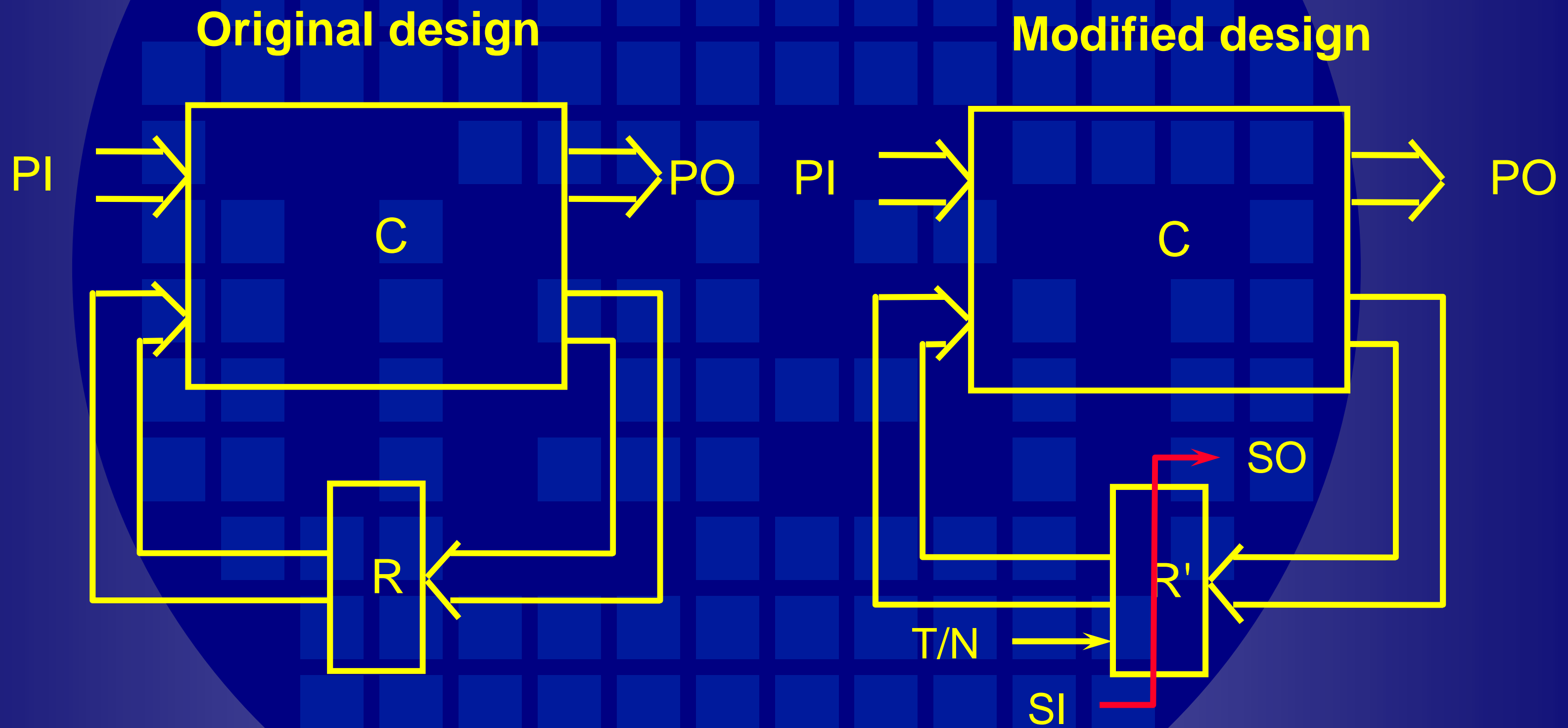
Example of ad hoc techniques

Insert test point



Scan System



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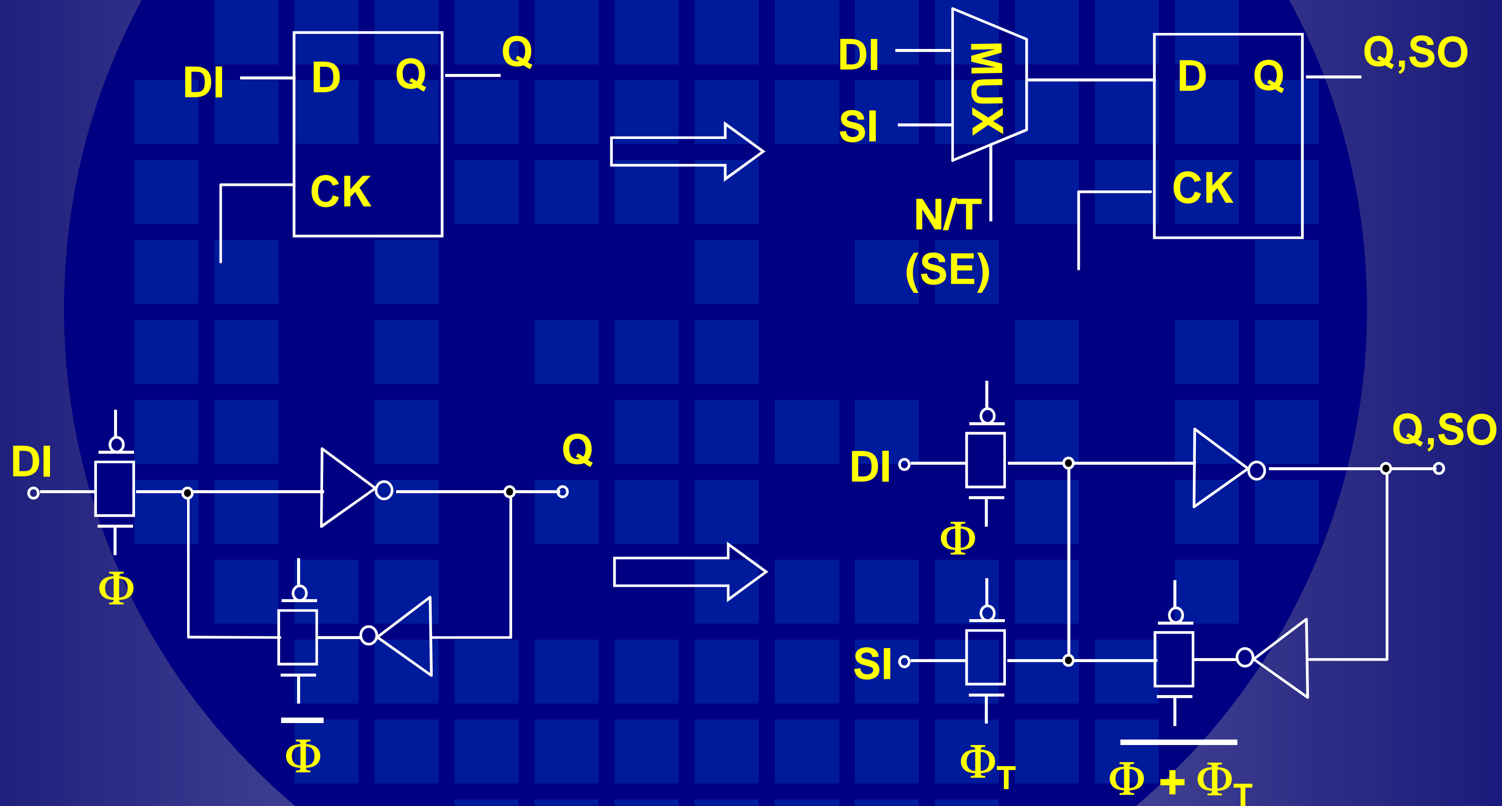
Scan Cell Design



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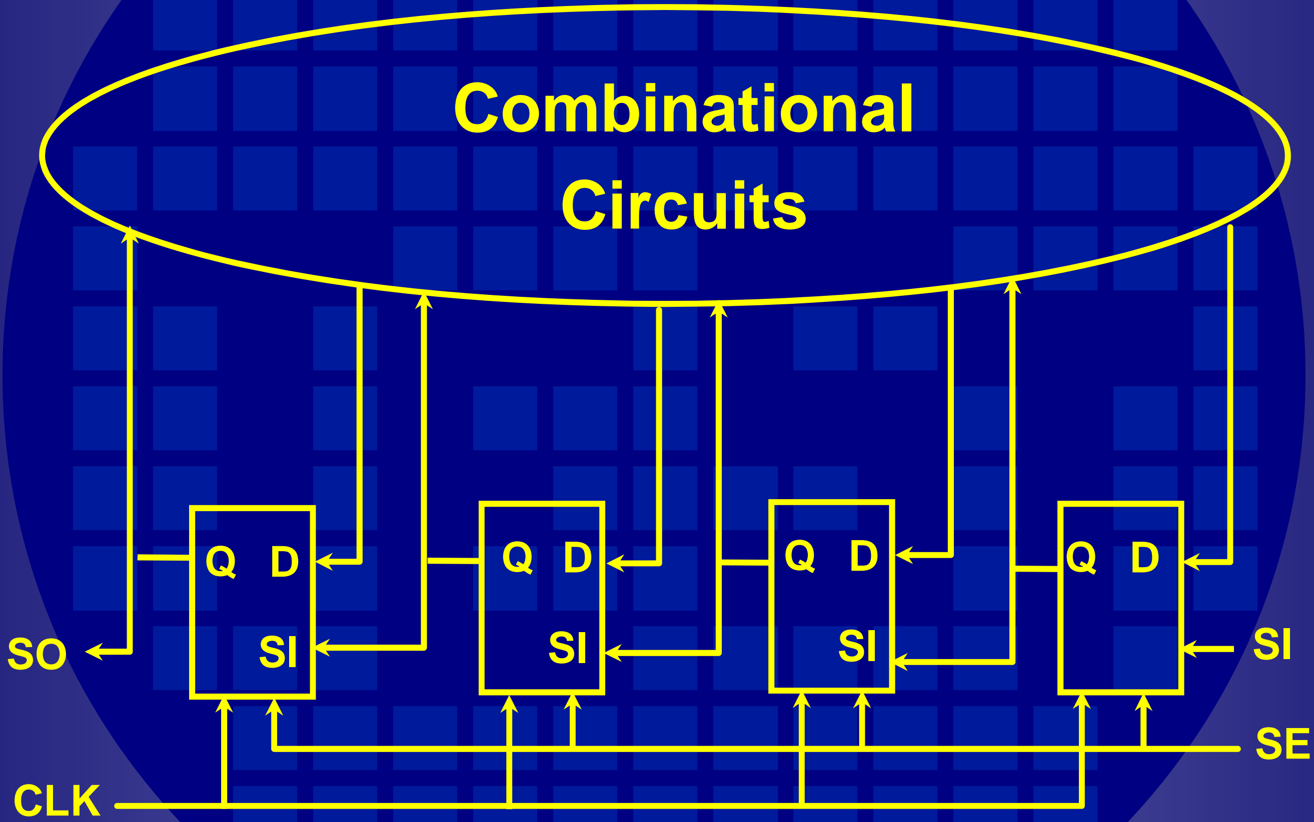
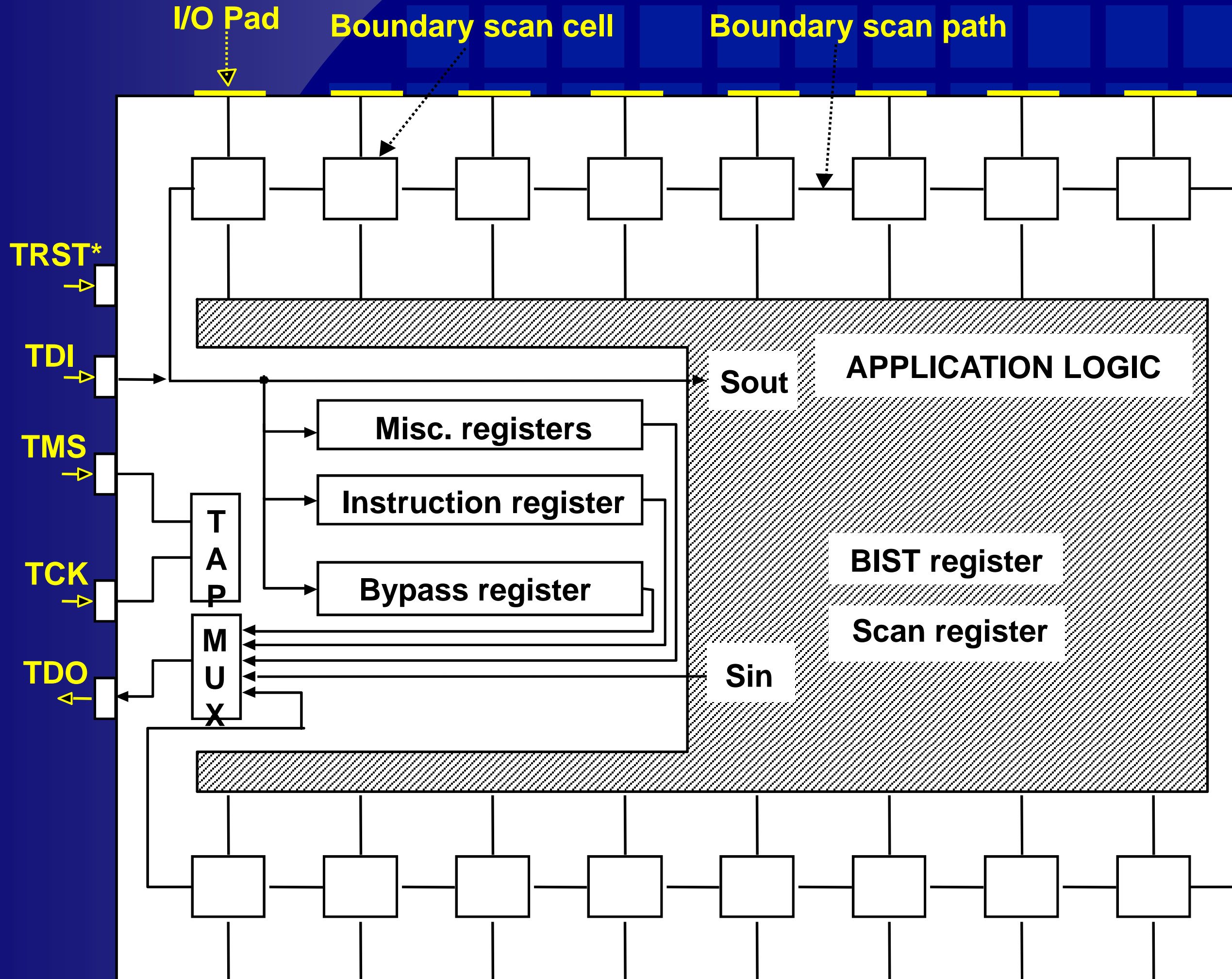
Scan Register

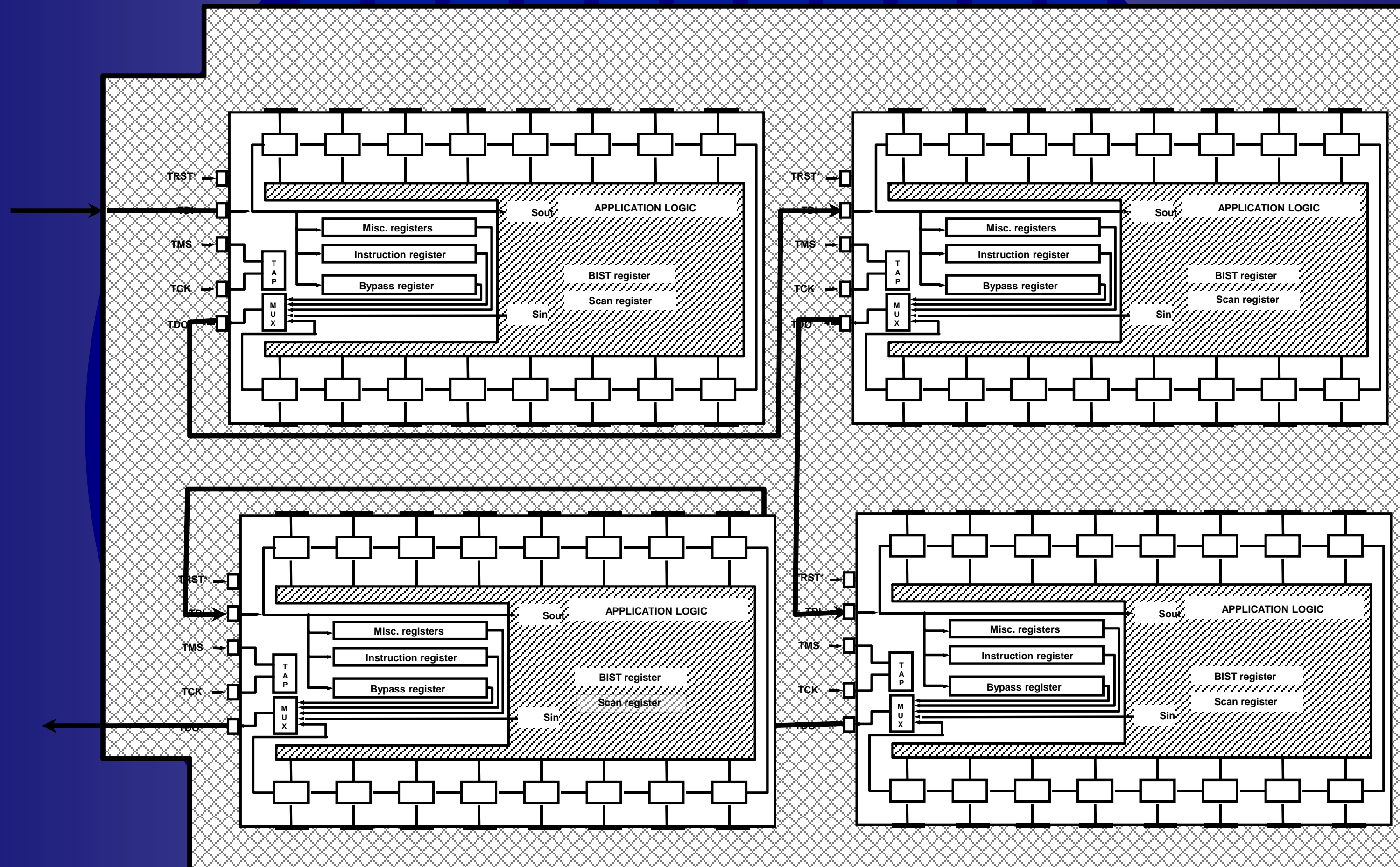


Boundary Scan



TRST*:Test rest (Optional)
TDI: Test data input
TD0: Test data output
TCK: Test clock
TMS: Test mode select

Boundary Scan (Cont.)



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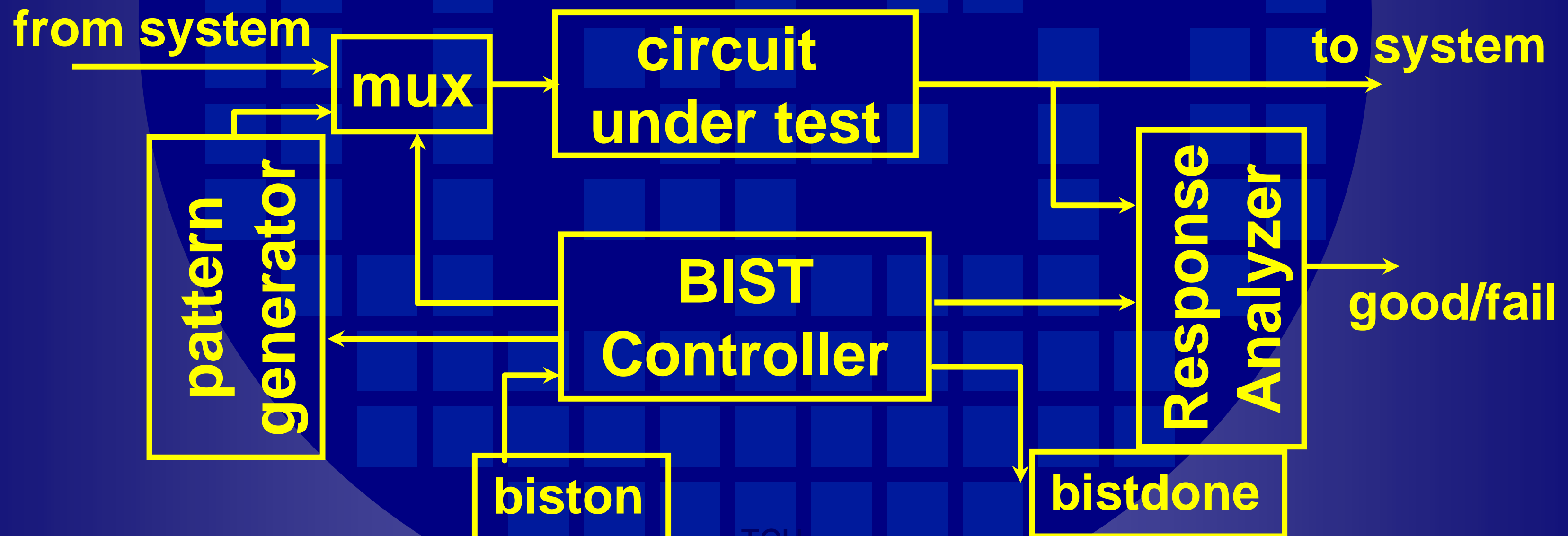
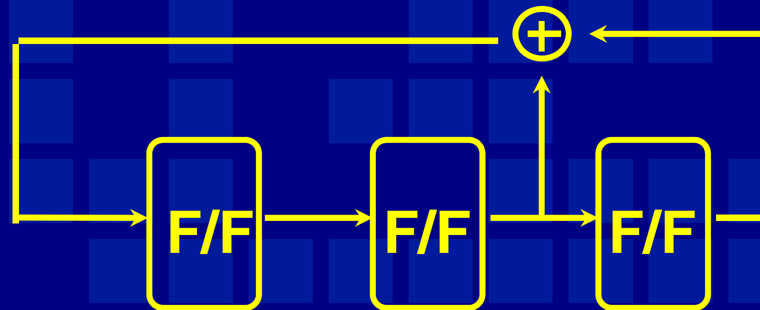
Built-In-Self Test (BIST)

- Places the job of device testing inside the device itself
- Generates its own stimulus and analyzes its own response



Built-In-Self Test (BIST) (cont.)

- Two major tasks
  - Test pattern generation
  - Test result compaction
- Usually implemented by linear feedback shift register



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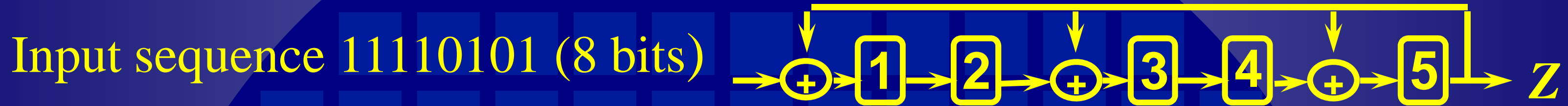
Signature Analyzer (SA)

Input sequence 11110101 (8 bits)



$G(x) = x^7 + x^6 + x^5 + x^4 + x^2 + 1$

$P(x) = 1 + x^2 + x^4 + x^5$

Time	Input stream	Register contents	Output stream
0	1 0 1 0 1 1 1 1	0 0 0 0 0	← Initial state
1	1 0 1 0 1 1 1	1 0 0 0 0	
.	.	.	
.	.	.	
5	1 0 1	0 1 1 1 1	
6	1 0	1 0 1 1 1	1
7	1	0 1 0 1 1	0 1
8		0 0 1 0 1	1 0 1

Remainder
$R(x) = x^2 + x^4$

Quotient
$1 + x^2$

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Signature Analyzer (SA) (cont.)

$$P(x): x^5 + x^4 + x^2 + 1$$
$$\times\ Q(x): x^2 + 1$$

$$x^7 + x^6 + x^4 + x^2 + x^5 + x^4 + x^2 + 1$$
$$= x^7 + x^6 + x^5 + 1$$

$$P(x)Q(x) + R(x) = x^7 + x^6 + x^5 + x^4 + x^2 + 1 = G(x)$$

Prob. of aliasing error = $1/2^n$

where n is # of FFs

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Automatic Test Equipment (ATE)
Flow

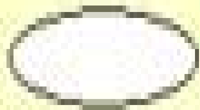
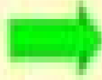
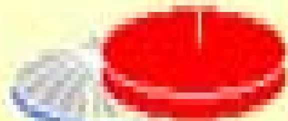
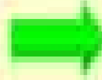
Taping

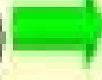
Grinding + Polish

Wafer Mount

Detaping

Sawing



Automatic Test Equipment (ATE)

Wafer Laminater

Automatic Test Equipment (ATE)

Wafer Backside Grinder

NCUE

Automatic Test Equipment (ATE)

Wafer Mounter

NCUE

Automatic Test Equipment (ATE)

Auto Dicing Saw

Automatic Test Equipment (ATE)
Auto UV Irradiation

Automatic Test Equipment (ATE)

Die Attach

Automatic Test Equipment (ATE)

Handler