**Final Examination Sheet**

Spring Semester, 2021, Dept. of Electronics Eng., National Changhua Univ. of Edu.

Course：***IC Testing*** Date：2021/6/21 (Mon.) Time：09:20~11:00 Place：Online (Google Meet)

***Note***: You can answer your exam by one of the following steps:

1. Please full-in or paste your answer by drafting using PowerPoint or Excel, transfer to pdf, name the file using your Reg.No and email to [tch@cc.ncue.edu.tw](mailto:tch@cc.ncue.edu.tw) by 11:20am.
2. Otherwise, you can write down your answers on paper and have a picture by camera, (paste them to a winword file, transfer to pdf), name the file using your Reg.No, and then email to [tch@cc.ncue.edu.tw](mailto:tch@cc.ncue.edu.tw).

Reg. No.：\_\_\_\_\_\_\_\_\_\_\_\_\_\_ Student’s Name：\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

1. TRUE OR FALSE (Mark ○ or X, 20%):

( ) 1. Test compression guarantees that the test set won’t be distorted or changed with a fewer size.

( ) 2. Boundary Scan (IEEE1149.1) can be applied for programming EEPROMs.

( ) 3. 0-1 march test detects more faults than.

( ) 4. To test the 4-way bridge fault A>B@0 between gates A and B, A and B are justified by 1 and week 1 (w1) and propagate 1 and w1/0, respectively.

( ) 5. -power model can be fit to most continuous functions within a local period.

( ) 6. The ‘slow’ in a ‘slow-fast-slow’ delay test is to make sure correct input and output of initial vector and response respectively.

( ) 7. A golden test proves that two products under test are good if their outputs are the same with the same input.

( ) 8. High-acceleration life test (HALT) is applied to screen out the early failure.

( ) 9. IC test can be fully saved if a fault tolerant mechanism is built in.

( ) 10. The frequency of an oscillating ring connected by 17 inverters will be reduced when the delay time of all inverters increase.

1. MULTIPLE CHOICE (Choose the best one, 20%):

( ) 1. Except 20 redundant faults, 72 of 80 non-redundant faults can be tested. Test efficiency= (A) 72% (B) 80% (C) 90% (D) 100%.

( ) 2. Which is not a simple codes? (A) AN codes (B) Hamming codes (C) RS codes (D) Berger codes.

( ) 3. How many bits can be corrected if Hamming distance d=8? (A) 1 (B) 2 (C) 3 (D) 4.

( ) 4. The most popular test for ADC is to test its (A) offset (B) nonlinearity (C) jitter (D) dynamic range.

( ) 5. The aliasing (false negative) rate of a 10-bit LFSR compressor is about (A) 10% (B) 1% (C) 0.1% (D) 0.01%.

( ) 6. Which diagram shows the working boundaries of products? (A) I-V (B) Space-Time (C) Shmoo (D) ladder diagram.

( ) 7. The most popular design for testability in industry is (A) Scan chains (B) MBIST (C) IDDQ monitor (D) ESD.

( ) 8. Assume the block error rate (BLER=) is measured in a frequency , the MTBF of the block will be (A) (B) (C) (D).

( ) 9. Backtracking of a recursive subprogram needs to (A) recover global data (B) recover local data (C) backtracing (D) backpropagation.

( ) 10. Which is a tool for testing? (A) Virtuoso (B) ICC (C) HFS (D) TetraMax.

1. QUESTIONS (60%):
2. Assume the jitters of a phase-lock-loop (PLL) is in a normal distribution. The root-mean-square jitter () will be approaching to its standard deviation when the independent measurement count *n* increases. However, the peak-to-peak jitter () will depend on *n*. According to the document at <https://www.sitime.com/api/gated/AN10007-Jitter-and-measurement.pdf>, how long is it to test a -PLL in a measuring rate? (10%)
3. Design an LFSR in the external type according to the primitive characteristic polynomial, (10%).
4. Encode input message word D[3:0] with three parities P[2:0] to a codeword C[7:1]={D[3:1], P[2], D[0], P[1], P[0]} in Hamming Codes using three RTL codes ‘assign P[ ] =’ in Verilog (10%).
5. Three march test algorithms are given as zero-one:, read-after-write: , and check-board: , where *t* is a toggling value. Assume the address count is N. Fill in the table for comparison. (10%) (Note: 10 blanks)

|  |  |  |  |
| --- | --- | --- | --- |
| March tests | Checkboard | Zero-one | Read-after-write |
| Algorithm |  |  |  |
| #Cycles |  |  |  |
| Stuck-at faults |  | V | V |
| Retention faults |  |  | X |
| Neighbor faults |  |  |  |

1. A, B are 16-bit integers. Design a parallel-decoded triple-modular redundant (TMR) for the addition, A+B. Hint: assume three sums are separately , , and . Multiple-bit comparators and multiplexers can be directly applied. (10%)
2. (a) Explain why a simulation in traditional HSPICE is called a fresh simulation? (5%)  
   (b) What’s differences between HALT and Burn-in ? (5%)