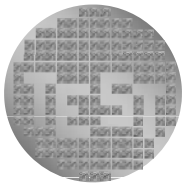

VLSI Test

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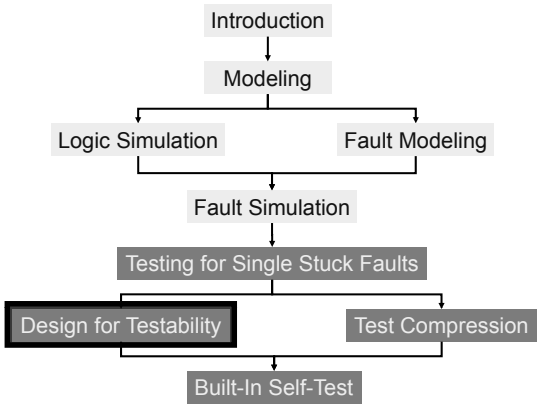
2016/03/28

Syllabus & Chapter Precedence

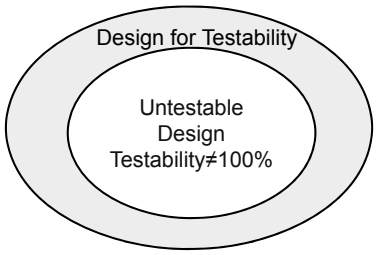


Testability

1. Controllability:
   - The ability (probability, time, or cost) to activate the fault.
2. Observability:
   - The ability (probability, time, or cost) to detect the error response.

DFT

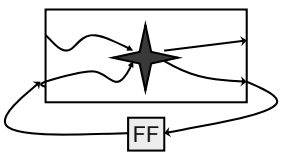
Design for Testability



Testable Design

Usual Causes to Untestability in SSF Model

1. Combinational Circuits:
   - Reconvergent Fanout and Self-masking
   - Redundant Circuits
2. Sequential Circuits:
   - Uncontrollable at PPI (Pseudo Primary Input)
   - Unobservable at PPO (Pseudo Primary Output)

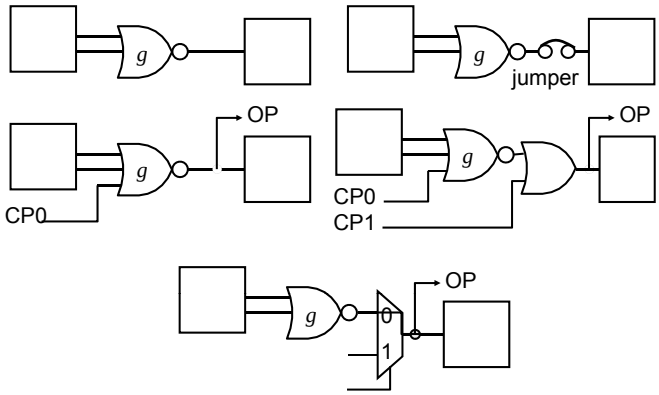


Ad Hoc for Testability Techniques

頭痛醫頭，腳痛醫腳

1. Test Points
2. Initialization (Reset)
3. Monostable Multivibrators (1-shots)
4. Oscillators and Clocks
5. Counters/Shift Registers
6. Partitioning Large Circuits
7. Logical Redundancy
8. Breaking Global Feedback Paths

Employing Test Points

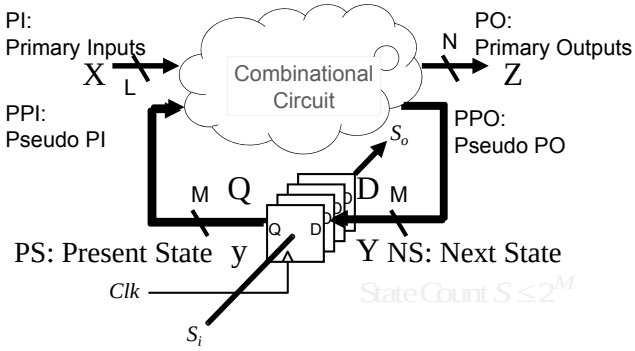


Scan Methodology

1. Integrated Scan
   - Serial Scan
     1. Serial Integrated Scan
        - Full (Serial Integrated) Scan
        - Partial (Serial Integrated) Scan
     2. Isolated Serial Scan
   - Non-Serial Scan
2. Boundary Scan

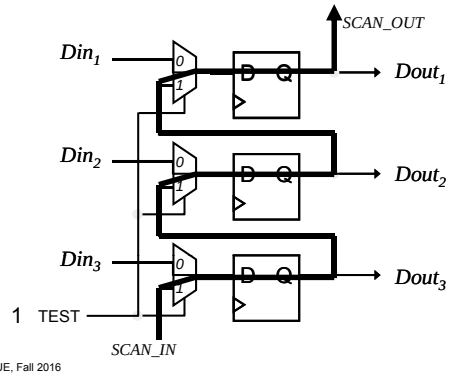
Huffman Model for a Typical Scan Circuit

Single Clock, Synchronous, DFF-based



Basic Scan Cells

MDFF, Multiplexed D-Flipflop



Scan Cell Insertion in HDL

```
module ckt(Clk, input, output);
…
leftmodule  (Clk, D2, …);
DFF  D2(Clk, D1, Q2);
 rightmodules  (Clk, Q2, …);
…
endmodule
```

→

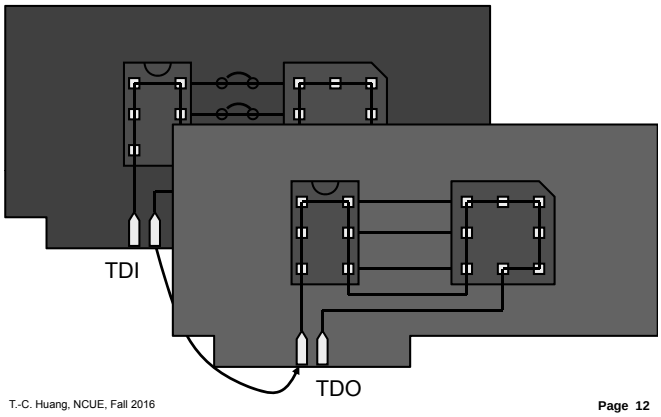
```
module scan_cell (TEST, Clk, Di, Do, Si, So);
…
mux (TEST, Di, Si, Mo);
DFF (Clk, Mo, Do);
assign So=Do;
endmodule

Module scan_ckt(TEST, Clk, input, output, Si, So);
…
assign  Si2=So1;
leftmodule (Clk, D1, …);
scan_cell  SC1(TEST, Clk, D1, Q1, Si2, So2);
 rightmodules (Clk, Q1, …);
…
assign So=Son;
endmodule
```

Test Synthesis

Boundary Scan

Basic Concept



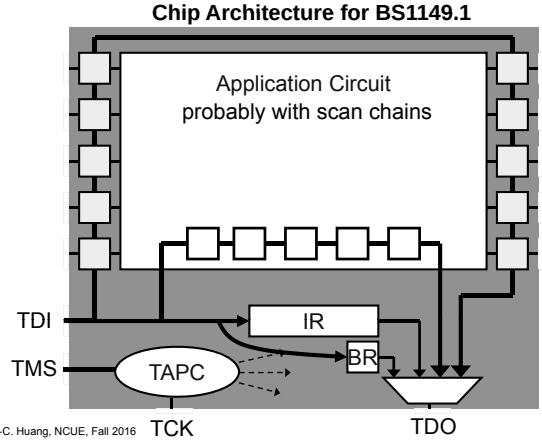
Boundary Scan

Background

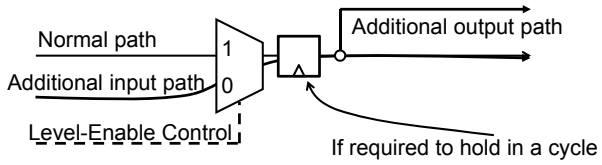
1. Joint Test Action Group (JTAG) Boundary Scan Standard, 1988
2. IEEE P1149.1 Testability Bus Standard (Proposal), 1989
3. Basic Structure:
   - TAP (Test Access Port) Controller
   - Registers: IR (Instruction Register) and BR (Bypass Register)
   - Extra Pins:
     - TMS (Test Mode Singal)
     - TCK (Test Clock)
     - TDI (Test Data Input)
     - TDO (Test Data Output)

Boundary Scan

Chip Architecture for BS1149.1

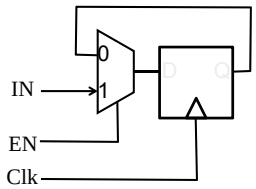


Path-Oriented Scan Cell Design



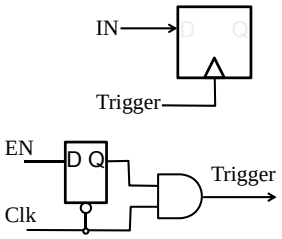
Conditional Activation

(1) Level-Enable Distribution



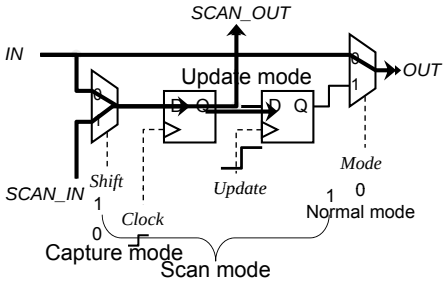
(+) High speed without skew and glitch
(-) a multiplexer overhead

(2) Gated-Clock Distribution



(-) Careful clock-gating required
(-) Gated clock skewed ➔ slow
(+) Directed clocking

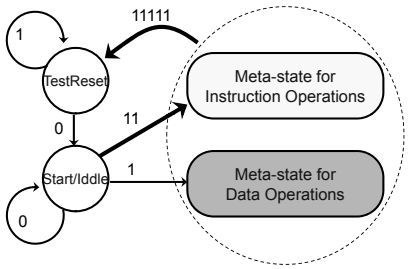
A Basic Boundary Scan Cell



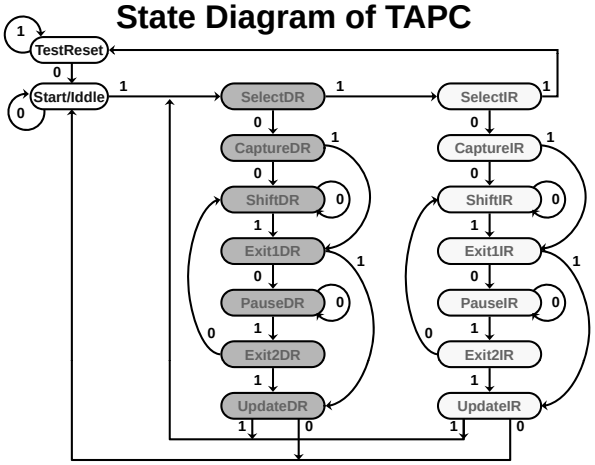
- Can update PIs (capture POs) simultaneously for detecting delay response.
- Can be used both as input and output boundary scan cells.

Basic Test Access Controller

A Synchronous Finite State Machine with 2X8 States



State Diagram of TAPC



Boundary Scan

Exercise with TI BS1.0

1. Exercise and trace some examples using TI Scan Educator 1.0
2. Write the basic TMS sequence for applying a pattern and detecting the result to a circuit under test (CUT) originally with 4 pins.
   Hint: Initialization, Scanning in 4 bits, Update, Capture, Scanning out 4 bits, Update.

Boundary Scan

Homework #1

1. Design an RTL code of a 3-bit adder in Verilog
2. Wrap it with 3x2+4 boundary scan cells
3. Design clock-gating circuit from UpdateEN to Update
4. Design a finite state machine for the TPC
5. Write a basic TMS sequence for applying 2 patterns and detecting the result to the circuit under test (CUT) originally with 10 pins.
6. Simulation in ModelSim
7. Submit the Verilog Code and a report with snapped figures to my email box by 2016/5/1