Sample and Reviews on Final Examination (Online)

Fill-in or Paste your Answer, Transfer to PDF and Email to me (tch@cc.ncue.edu.tw) by 11:30

Course：***IC Testing*** Date：2021/6/7 (Mon.) Time：09:20~11:00 Place：Online

Reg. No.：_____ Student's Name：_____

I. TRUE OR FALSE (Mark ◯ or X, 20%):

(◯) 1. The 'slow' in a 'slow-fast-slow' delay test is to make sure correct input and output of initial vector and response respectively.

(◯)2.0-1 march test ⇑ $w0$⇑ $r0$⇑ $w1$⇑ $r1$ detects more faults than ⇑ $w0r0$⇑ $w1r1$.

(◯) 3. To test the 4-way bridge fault A>B@0 between gates A and B, A and B are justified by 1 and week 1 (w1) and propagate 1 and w1/0, respectively.

(◯) 4. α-power model can be fit to most continuous functions within a local period.

(X) 5. IC test can be fully saved if a fault tolerant mechanism is built in.

(◯) 6. The frequency of an oscillating ring connected by 17 inverters will be reduced when the delay time of all inverters increase.

(X) 7. A golden test proves that two products under test are good if their outputs are the same with the same input.

(X) 8.High-acceleration life test (HALT) is applied to screen out the early failure.

(X) 9. Test compression guarantees that the test set won't be distorted or changed with a fewer size.

(◯) 10. Boundary Scan (IEEE1149.1) can be applied for programming EEPROMs.

II. MULTIPLE CHOICE (Choose the best one, 20%):

(A) 1. Which program reads a language and constructs efficient data structures: (A) parser (B) loader (C) interpreter (D) script.

(A) 2. Backtracking of a recursive subprogram needs to (A) recover global data (B) recover local data (C) backtracing (D) backpropagation.

(D) 3. Which is a tool for testing? (A) virtuoso (B) design compiler (C) HFS (D) tmax.

(B) 4. How many bits can be corrected if Hamming distance d=5? (A) 1 (B) 2 (C) 3 (D) 4.

(C) 5. Except 20 redundant faults, 72 of 80 non-redundant faults can be tested. Test efficiency= (A) 72% (B) 80% (C) 90% (D) 100%.

(C) 6. Which is mainly responsible for transistor-level simulation? (A) Encounter (B) Debussy (C) HSPICE (D) Virtuoso.

(A) 7. The most popular design for testability in industry is (A) Scan chains (B) MBIST (C) IDDQ monitor (D) ESD.

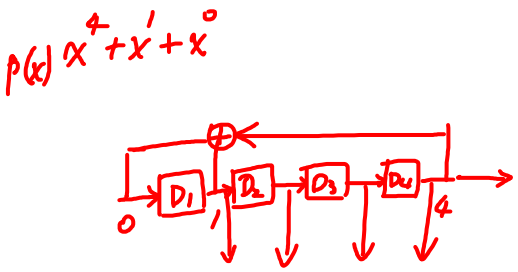
(B) 8. The most popular test for ADC is to test its (A) offset (B) nonlinearity (C) jitter (D) dynamic range.

(C) 9. TMR corrects the fault by accepting the (A) average (B) minority (C) majority (D) last.

(C) 10. Which diagram shows the working boundaries of products? (A) I-V (B) Space-Time (C) Shmoo (D) ladder diagram.

III. QUESTIONS (120%, at most 60% adopted):

1. Design an LFSR in the external type according to the primitive characteristic polynomial, $p^*(x)$ or $p(x) = x^4 + x + 1$ (10%).



2. Encode input message word D[3:0] with three parities P[2:0] to a codeword C[7:1]={D[3:1], P[2], D[0], P[1], P[0]} in Hamming Codes using three RTL codes 'assign P[ ] =' in Verilog (10%).

```
assign P[0] = D[0] ^ D[1] ^ D[3];
assign P[1] = D[0] ^ D[2] ^ D[3];
assign P[2] = D[1] ^ D[2] ^ D[3];

assign E[0] = P[0] ^ D[0] ^ D[1] ^ D[3];
assign E[1] = P[1] ^ D[0] ^ D[2] ^ D[3];
assign E[2] = P[2] ^ D[1] ^ D[2] ^ D[3];
```

P2	P1	P0	
0	0	0	
0	0	1	P[0]
0	1	0	P[1]
0	1	1	D[0]
1	0	0	P[2]
1	0	1	D[1]
1	1	0	D[2]
1	1	1	D[3]

3. Give the English and Chinese terms to explain the three cycles in the bathtub curve (6%). How can we accelerate the first cycle? (4%)

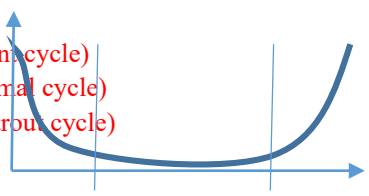
(I) 三個時期

(1) 早夭期 (Infant cycle)

(2) 正常期 (Normal cycle)

(3) 損耗期 (Wearout cycle)

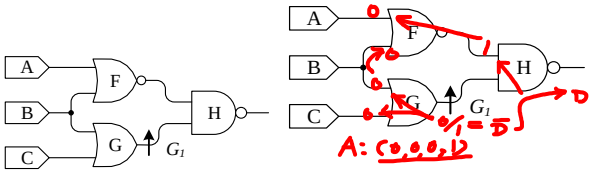
(II) Burn-in (崩應)

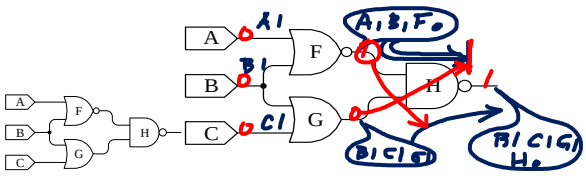


4. Three march test algorithms are given as zero-one: ⇑ $w0$⇑ $r0$⇑ $w1$⇑ $r1$, read-after-write: ⇑ $w0r0$⇑ $w1r1$, and checkboard: (⇑ wt⇑ rt)t(⇑ wt⇑ rt) , where t is a toggling value. Assume the address count is N. Fill in the table for comparison. (10%) (Note: 10 blanks)

March tests	Checkboard	Zero-one	Read-after-write
Algorithm	(⇑ wt⇑ rt)t(⇑ wt⇑ rt)	⇑ w0 ⇑ r0 ⇑ w1 ⇑ r0	⇑ $w0r0$⇑ $w1r1$
#Cycles	4N+1	4N	4N
Stuck-at faults	V	V	V
Retention faults	V	V	X
Neighbor faults	V	X	X

5. Given the fault list of the following circuit as L_f = {A_0, A_1, B_0, B_1, C_0, C_1, F_0, F_1, G_0, G_1, H_0, H_1} where G_x means gate G stuck-at-x fault, (1) justify and propagate to find the test pattern T_{G1} of G_1. (2) Then do deductive fault simulation to collect all testable faults of T_{G1}. (3) Calculate the fault coverage of T_{G1}, FC(T_{G1}, L_f). (20%)





FC = 4/12 = 33.3%

6. Explain the following terms: (a) Shmoo Plot, (b) MTTF (10%)

(a) The Shmoo plot is a diagram to show the working range, usually with two axes of supply voltage and working temperature.

(b) MTTF means the mean time from a healthy state to failure, which is similar to MTBF, from failure to failure. The units are usually in years, or hours.

7. (a) Explain why a simulation in traditional HSPICE is called a fresh simulation? (5%)
(b) What's differences between HALT and Burn-in ? (5%)

(a) The simulation in tradition SPICEs including HSPICE is usually called the fresh simulation because they won't consider the aging time.

(b) HALT is to pretest the life in a very high temperature for providing rough parameters for later aging model tuning.

However, the burn-in is to accelerate the early aging effects in the infant cycle to screen out the non-reliable products.

8. (a) Some paper claimed that a single sampling for one normal-distributed parameter can get a mean value result with only a ± 0.01 error. However, most people have known that the deviation is also about 0.01. How is the confidence level of the experiment? (5%)

(a) Since $\sigma = 0.01$ and $\text{error}(n = 1) = 0.01$, so z=1, the confidence level = 95%.

(b) To achieve an error less than σ/k (k is a positive integer) in a $z\sigma$ precision, what is the least sample size? (5%)

The sample size will be $n = \left(\frac{z\sigma}{\sigma/k}\right)^2 = (zk)^2$.