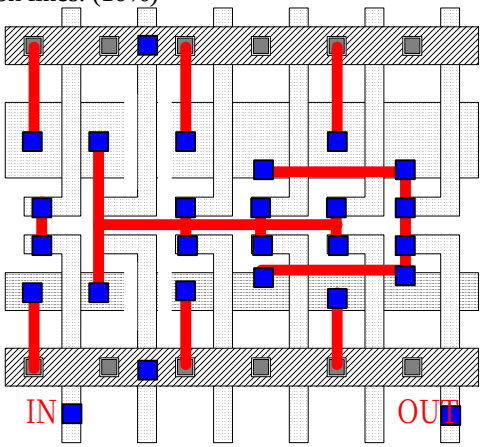
國立彰化師範大學電子系九十三學年第一學期期末考考卷

課目：數位 IC 設計 日期：2005/01/11(Tue.) 時間：1:00~2:40pm 地點：31303 老師：黃宗柱

1. Lay out a buffer with a stage ratio 1:3 (3 parallel inverters driven by an inverter) on the following SOG. Remember that you can use a turned-off transistor to split the diffusion lines. (10%)



2. Design a scan cell and then synthesize a full scan chain for the following circuit CUT to CUT_S0. (10%)

```
module   CUT(Clk, A, B, C, E);
input    Clk, A, B, C;
output   E;
dff      FF1(.clk(Clk), .q(E), .d(F));
nand     g1(F, A, B), g2(G, F, C);
nor      g3(H, I, G);
dff      FF2(.clk(Clk), .q(I), .d(H));
endmodule
module   SC(Clk, SE, Out, Si, Di);
input    Clk, Si, Di;
output   Out;
mux      g1(SE, D, Si, Di);
dff      f1(.clk(Clk), .q(Out), .d(D));
endmodule
module   CUT(SE, Si, So, Clk, A, B, C, E);
input    SE, Si, Clk, A, B, C;
output   So, E;
SC       FF1(Clk, SE, E, Si, F);
nand     g1(F, A, B), g2(G, F, C);
nor      g3(H, I, G);
SC       FF2(Clk, SE, I, E, H);
assign   So=I;
endmodule
```

3. Neglecting the jitters, skews, setup time and clock-to-Q times, let the propagation time of Finite State Machine $Z_i=M_i(X_i)$ be t_{QCi}. What's the propagation time of $Z_4=M_4(M_3(M_1(X_1), M_2(X_2)))$? How is the IP rule used to reduce it? (10%)

1. $t_{Qc4}=max(t_{Qc1}, t_{Qc2})+t_{Qc3}$
2. The IP design rule can constrain that the paths for PIs to FFs should be reduced, i.e., each FF is placed near to the PIs so that $t_{Qc4}=max(t_{Qc1}, t_{Qc2}, t_{Qc3})$.

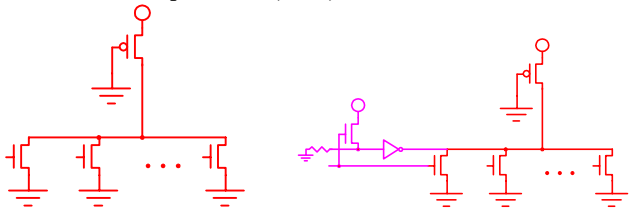
4. Give at least 5 issues for IP reuse. (10%)
Such as IP authorization, IP Testing, IP Interface/Platform, Area, Power dissipation, Performance Impact, etc.

5. What are the four units in a typical processor? (10%)
IOU, MU, CU, Datapath

6. Draw a digital IC design flow using tools from the CIC. (10%)
e.g., Design→Presim(NCSim)→Test synthesis(Syntest)→Preverification(NCSim)→Gate-Level Synthesis(Synopsys)→Physical Synthesis→Postsim(NCSim)→Tapein

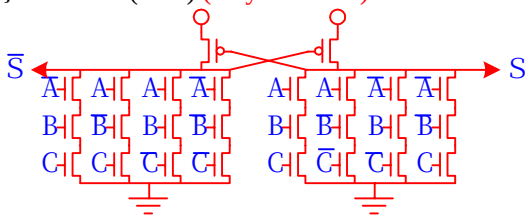
7. Explain what are bus contention and floating? How can we prevent them?(10%)
Contention includes any confliction of input values of a wired logic, especially for the connection of tri-state buffers. When the inputs are all with a high impedence value, the wired connection is then floating.

8. What structure do we usually use to implement a many-input NOR gate? What disadvantage does it have? How can we improve it? (10%)



NMOS. The sizes of n devices are designed very narrow such that the fall time is large. The SFPL (source follower pull logic) will detect any coming-1 of the inputs and then feed forward to drive the output.

9. Draw a CVSL schematic of a full adder, {Co, S}=A+B+Ci.(10%) (only S shows.)



10. Draw the basic SRAM architecture introduced in this course. (10%)